

White Paper

Fuze Electronics Miniaturization

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(1) Statement of Requirements

The army needs a robust electronic module that will sustain high shock levels such as 20,000 G's and 100,000 G's in a miniaturized form and at an attractive cost.

(2) Description of Core Capabilities and Technology

Peter C. Salmon, LLC is a consulting business providing creative solutions in the electronic product arena. Multiple conference presentations and publications document a history of

advanced system designs employing novel packaging techniques. A forerunner of the proposed technology, called "Buckled Pillar", has been advanced in multiple technical journals and web publications [see section (8)], but has not yet been reduced to practice.

(3) Proposed Technology Solution

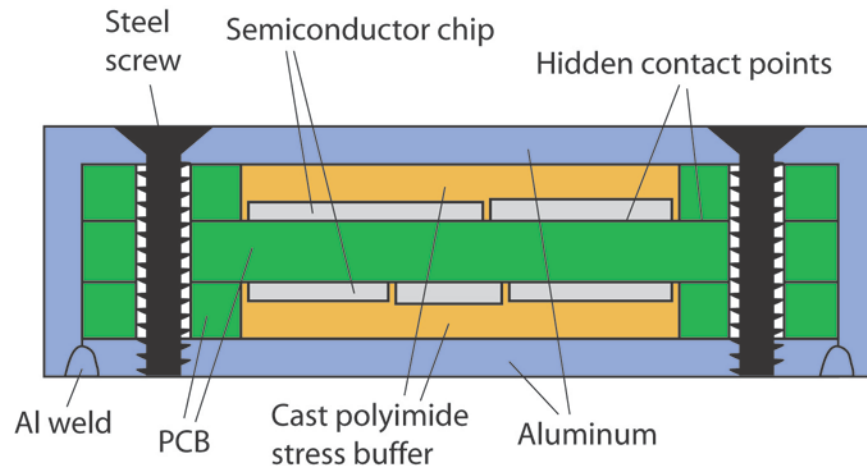


Figure 1

Figure 1 is a schematic side view of a miniaturized fuze electronics module that can withstand high G forces. The degree of miniaturization is approximately 5X over an assembly using individually packaged semiconductor chips. Approximate calculations will show that this design can withstand accelerations of over 100,000 G's. This is a consequence of the material selection and the rugged form factor. However, a number of material incompatibilities must be overcome, to be further discussed.

The preferred printed circuit board (PCB) substrate material is common FR4 because of its availability and cost, and its reasonable coefficient of thermal expansion (CTE). Aluminum is used for the shell enclosure, having a good strength to weight ratio and modest thermal compatibility problems. Cast polyimide is used for the stress buffer adjacent the semiconductor chips; it retains excellent physical properties at temperatures up to 150°C and can be cast into the available space. It fills voids and provides desirable cushioning of integrated circuit (IC) chips in x, y, and z-directions. A novel method for providing contact points between chips and PCBs and between mating PCB surfaces will be further described.

Double Assembly Method

A "double assembly" method is proposed. The first assembly employs steel screws, enabling a module test with no cast polyimide present. Any defective components are identified and replaced. After electrical validation, the polyimide is cast in place, and the module is re-assembled with screws. The screws hold the assembly together and provide a path to external heat sinks during the process of welding the outer shell closed. Finally, the screws may be removed and the screw holes also closed by welding, thus creating a quasi-hermetic package capable of meeting more stringent requirements than those of Mil Std 331C. This version of the assembly is also tamper-resistant because of the physical challenge in accessing the module. Tamper proofing may be provided by electronically disabling the device in the absence of a suitable access code applied using a preferred covert means, and by detecting unapproved device access using further covert means.

This assembly method is considerably more flexible than recent "Embedded Die Technology" approaches advanced by Imbera, Casio and others. Also, the proposed module does not use any solder, avoiding many solder-related reliability problems.

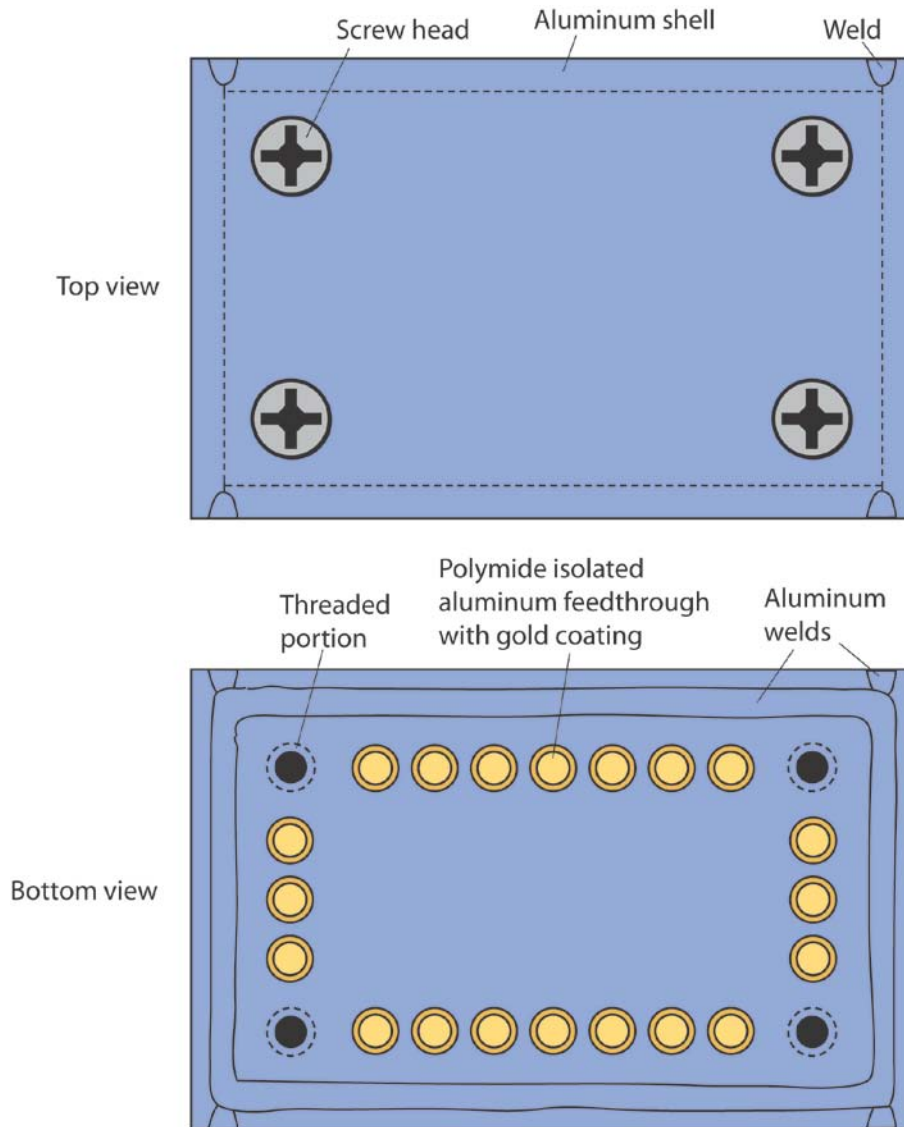


Figure 2. Top and Bottom View of Proposed Module

The module is connected to signals and power through gold coated contacts shown in the bottom view. The method of forming the polyimide-isolated feedthroughs will be described. As will be further discussed, the contact areas protrude slightly beyond the plane of the aluminum base.

Thermal Design

Thermal coefficients of expansion are provided in Table 1 below. Since the module is solder free, temperature variations may occur during storage, shipping, or operation but not during assembly. It is anticipated that the proposed modules will perform well across the mil-spec range of $-55^{\circ}\text{C} \leq T \leq 125^{\circ}\text{C}$, exceeding the requirements of Mil-Std-331C. The 1mm thick polyimide stress buffer is capable of absorbing thermally induced stress between the chips and the aluminum shell. Gold connections between the chips and the center PCB are also capable of adapting to thermally induced stress at that interface, to be further described.

The IC chips are cooled by conduction of heat to external module surfaces which may be cooled by air convection for example. Cooling fins may be added.

Electrical Design

Low impedance paths are provided for power and signals. These are redistributed at each PCB layer, to accommodate the various chip pinouts.

Structural Design

The module structure is inherently robust. Air gaps are eliminated using cast polyimide; thus the assembly behaves according to the mechanical properties of the bulk materials. Stresses are absorbed and dissipated through "controlled collapse", beginning with the polyimide stress buffer as the first material to yield. At each given thickness a maximum strain of 1% is assumed, judged to be a reasonable value for maintaining the physical integrity of the module.

The maximum G's are calculated in a direction orthogonal to the base of the module. Sophisticated 3D modeling can provide more accuracy, plus results at other orientations.

Material	E	ρ	CTE	Max op'g T	Thickness	Max G's	Order
Aluminum	70	2.70	23.1	660	1000	26	3
Copper	130	8.92	17.0	1085	1000	15	
Gold	78	19.3	14.2	1064	100	41	5
Tin	50	7.31	22.0	232	1000	6.9	
Indium	11	7.31	32.1	157	1000	1.5	
Silicon	47	2.33	2.6	~ 250	525	39	4
FR4	21	1.85	13.0	140	1575	7.3	2
Polyimide	6.3	1.42	16	~ 300	1000	4.5	1
Units	10^9 N/m²	10^3 kg/m³	10^{-6}W/m°C	°C	10^{-6}m	10^6G	

Table 1. Material properties and maximum G forces

Table 1 shows the order of "controlled collapse": polyimide first, then FR4, then aluminum, then silicon, and lastly the gold contacts. For comparison, some soft metals are included for evaluation of their stress buffering properties, also copper as an alternate material for the outer shell. For the chosen material set and orientation, a sustainable shock level of 4.5 million G's is calculated. The gold contacts will actually deform more readily than implied by Table 1, because they are limited in lateral extent, requiring a 3D model for an accurate prediction.

Calculation of Maximum G's

F = force, m = mass, A = area, t = thickness, Δt = change in thickness, a = acceleration, E = Young's modulus, ρ = density.

By the definition of Young's modulus, $F/A = E (\Delta t/t)$

Substituting $F = ma$ using Newton's second law of motion, and rearranging:

$$ma/A = E(\Delta t/t); a = E(\Delta t/t)A/m = E(\Delta t/t)(1/\rho t)$$

$$a = E/\rho(\Delta t/t)(1/t)$$

Assume maximum strain

$$\Delta t/t = 1\% = 0.01$$

$$a = 0.01 E/\rho(1/t)$$

Accordingly, as a useful approximation, a comparison of maximum accelerations shown in Table 1 can be calculated using E and ρ of the bulk materials, as well as their thickness t.

IC Chips

The module can accommodate a wide variety of IC chips, including digital, analog, RF, and mixed signal designs. Different semiconductor materials may be used, including silicon, GaAs, and SiGe as examples. If advanced chips employing through silicon vias (TSVs) become available, these can be integrated in stacked configurations, and the proposed architecture for fuze electronics can follow the trajectory of technology evolution. Also, because effective rework procedures are available, the number of die that can be integrated in a module is not limited by compound yield concerns.

Patent Pending

A patent application has been submitted on the apparatus and method described herein.

Discrete Components

Discrete devices such as capacitors, resistors, and inductors are preferably provided using arrays of such devices integrated onto IC chips and assembled in the standard manner shown in Figure 1. In some designs it may be useful to provide larger spaces between the IC chips, and attach surface mount components to PCBs using solder. These devices would subsequently be embedded in the cast polyimide material.

Miniaturization

By eliminating individual packages for each IC chip and also by employing flattened gold contacts, a space efficient structure is achieved that results in a highly compact module. The achievable miniaturization factor is estimated at 5X over more conventional packaging. However, this factor will not be accurately known until real examples are designed and prototyped using a given chip set. The author has studied buckled pillar assemblies [see Section (8)], that occupy only 5% of the volume of currently manufactured blade servers. Additionally, the module screws can be lengthened for attaching the module to a host surface, integrating the module with the system in a space-efficient yet mechanically robust manner that will contribute to miniaturization at the system level. Further, multiple modules containing the same or different circuits can be stacked in such a system, by appropriately configuring the layers.

Contact Points between IC Chips and PCBs

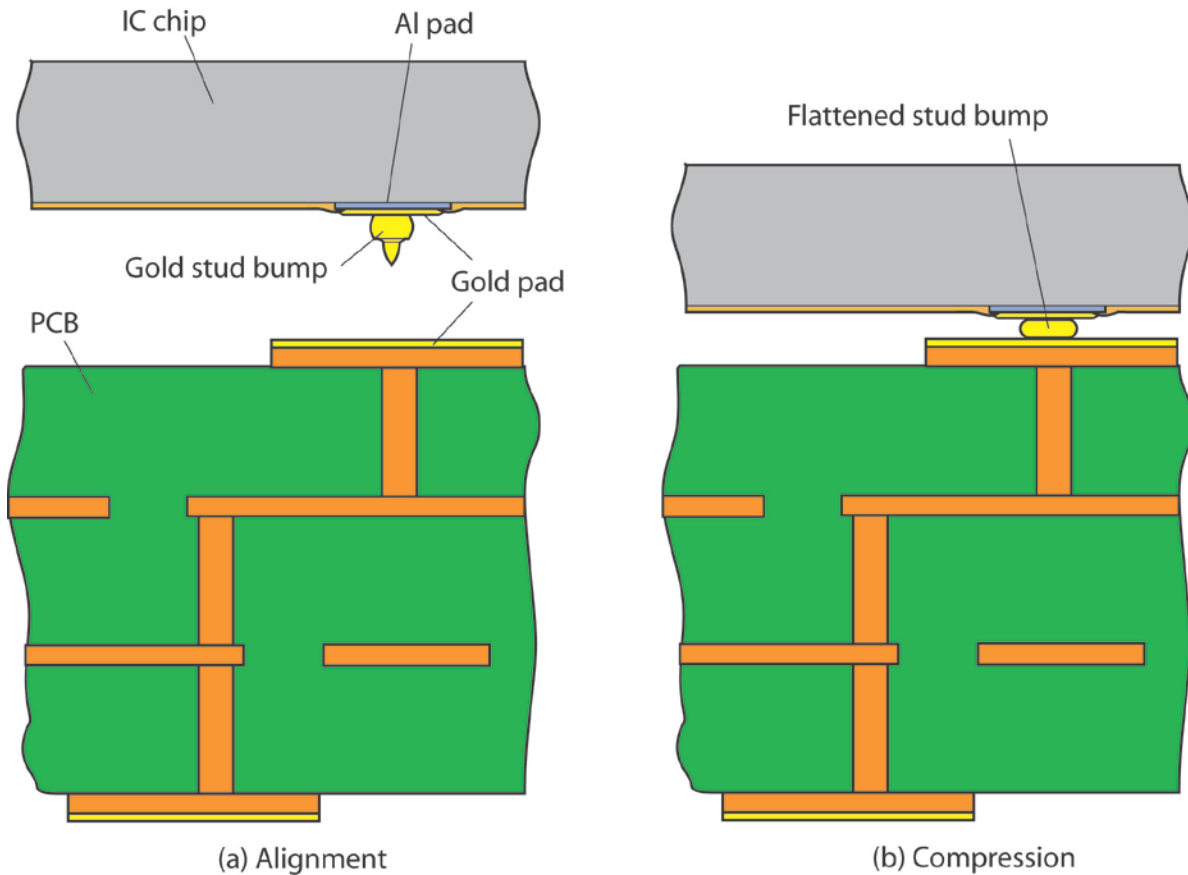


Figure 3. Alignment and bonding of contact points

Minimum sized gold stud bumps are formed at I/O pads of IC chips using standard stud bumping equipment and processes. They are also formed at some PCB pads, to provide electrical connections at opposing PCB surfaces.

In order to interface the fine structure of chip interconnections to the generally coarser structure of PCB interconnections, a fine-pitch PCB process is used. An example is available from the Microelectronics Division of Sierra Circuits in Sunnyvale, California. This capability includes 25 μm lines and spaces, 50 μm laser drilled vias, and 200 μm core via pitch. Other shops offering similar capabilities are also available.

Precision alignment and bonding of the IC chips to the PCB pads can be accomplished using assembly equipment such as provided by Finetech GmbH. Using split field optics, an alignment accuracy of a few micrometers can be achieved. For the proposed modules, alignment accuracy of $\pm 10 \mu\text{m}$ will be adequate, and this is currently available in production machines.

Figure 3(b) shows the effect of compressing the gold stud bump into a pancake form. Thus, the front side of each die is supported by an array of gold connections, and the back side is supported

by a thick layer of cast polyimide. One can imagine that lateral motion between the IC chip and the PCB (due to either shock or thermal mismatch) will cause both a rolling motion and a smearing action at the gold contact. This can be confirmed by computer modeling. If true, substantial lateral motions will be well tolerated.

Fabrication of Aluminum Base Plate with Polyimide-Isolated Feedthroughs

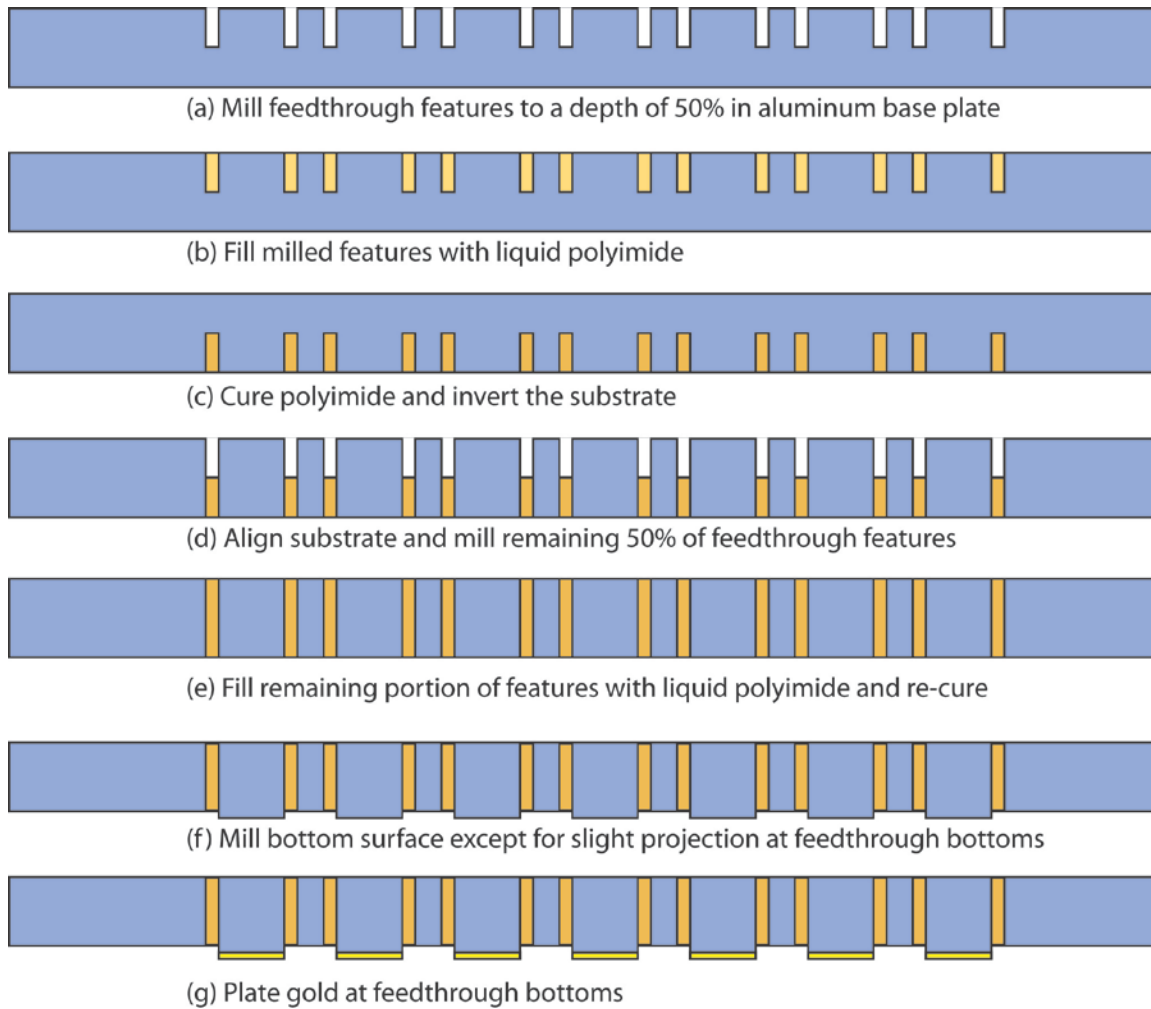


Figure 4. Fabrication Method for Polyimide-Isolated Feedthroughs

(4) Feasibility Assessment

The proposed modules employ standard materials including standard semiconductor chips, aluminum, FR4, cast polyimide, and gold-to-gold contacts. The fabrication processes are well known except for the process outlined in Figure 4. However, this process uses standard materials and well known capabilities such as milling, screen printing, electroless plating and polyimide curing; it is highly feasible. The fine-trace PCBs are not a fully mature technology, but they have been produced successfully for several years at Sierra Circuits. Other shops provide similar

capabilities. Accordingly, evaluation prototypes are considered eminently feasible. Volume production entails additional risks, but these are judged to be manageable.

(5) Costs

A cost model needs to be developed. Except for the cast polyimide the materials are commonly available and inexpensive, and the module will have an attractive bill-of-material (BOM) cost. It may be possible to substitute a less expensive potting material (such as a hydrophobic wax) for the polyimide, although its physical, electrical, and thermal properties are hard to match. The equipment requirements are generally modest, including screen printers, curing ovens, a milling machine, and an aluminum welder. However, the chip aligner/bonder is a sophisticated instrument and carries an associated cost. Gold stud bumping and electroless plating are available through service companies at competitive prices. For standardizing the thickness of the IC chips, wafer back-grinding services may be used; these are also widely available.

Following the first assembly, the module can be disassembled using a screw driver and a torque wrench tool for removing die by breaking the gold-to-gold contacts. This leads to a lower yielded cost because defective components are identified and replaced.

(6) Risk Assessment

We judge the highest risk to be cracking of the IC chips under either extreme shock conditions or extreme temperature stress. We believe that the proposed structure will sustain high shock levels, primarily due to the stress absorption properties of cast polyimide, but also from the novel support of the chips on malleable gold contact areas. To mitigate the risk of cracking, computer modeling of multiple configurations and orientations should be conducted. Similarly, thermal cycling limits should be validated using computer models. We do not foresee any other substantial risks.

(7) Technology Readiness

We recommend a three-month period of intensive computer modeling, followed by physical testing of prototype modules for an additional three months. Reliability testing should follow, and dependable modules are expected within 12 months of the start date, assuming test wafers are available.

(8) Other Related Projects

We have conceived of a similar technology for solder-free assembly of electronic modules under normal shock conditions. This approach is called "Buckled Pillar", or alternatively "Pillar-In-Well". An animation of the process is available at:

<http://www.electroiq.com/index/display/packaging-article-display/339446/articles/advanced-packaging/industry-news/2008/09/solder-free-connectors-using-buckled-pillars.html>

The primary lesson learned from this project is that most commercial and defense companies are reluctant to adopt new technology. To motivate the process of building prototypes and performing reliability studies there has to be a specific driver, such as generic fuze performance coupled with substantial miniaturization. Once these tests have been performed, the merits of the new technology will be apparent.

(9) Independent Testing Results

None are available at this time.

(10) References

See

<http://petersalmon.com>

for publications and patents, a section on 3D packaging, and Peter Salmon's bio.