



Novel SiP design concept: Stacked Copper BGA

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Outline

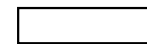
- Packaging concerns from the Technology Roadmap
- The copper advantage
- Heat interface solutions
- Copper BGA
- Stacked copper BGA
- Known good die testing and burn-in
- Conclusion

Technology Roadmap: ITRS 2003

(High performance category)

	2004	2007	2010
Max power, W/mm ² [4]	0.51	0.61	1.55
Package pincount [5], [6]	3,000	4,000	4,009
Cost, cents per pin	1.88	1.61	1.37

Manufacturable solutions exist



Manufacturable solutions are known



Manufacturable solutions are NOT known



[4] Power will be limited more by system level cooling and test constraints than packaging

[5] Pin counts will be limited for some applications by system level PWB cost impact

[6] The pin counts assume the signal to reference pin ratios will vary from 1:4 to 2:1 across different market segments



The copper advantage: thermal conductivity

	σ	Ratio
FR4	0.0030	1.0
Thermal grease	0.35	117
Solder	0.2-0.7	67-233
Silicon	0.98	327
Copper	3.9	1300

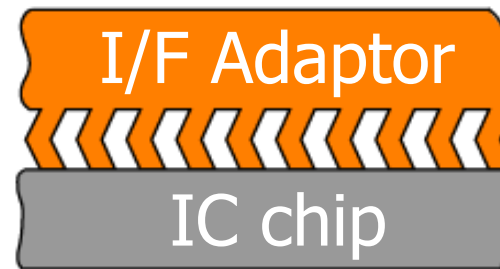
σ = thermal conductivity in W/cm^{°C}



Heat interface concepts



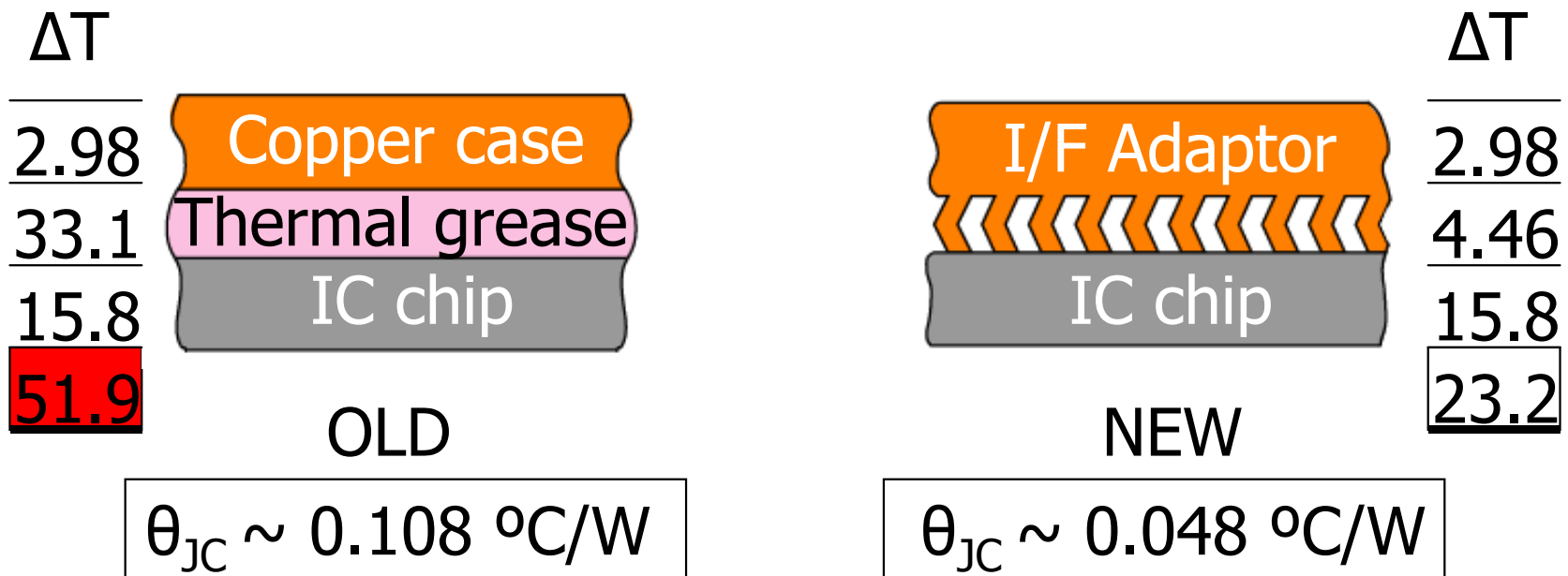
OLD



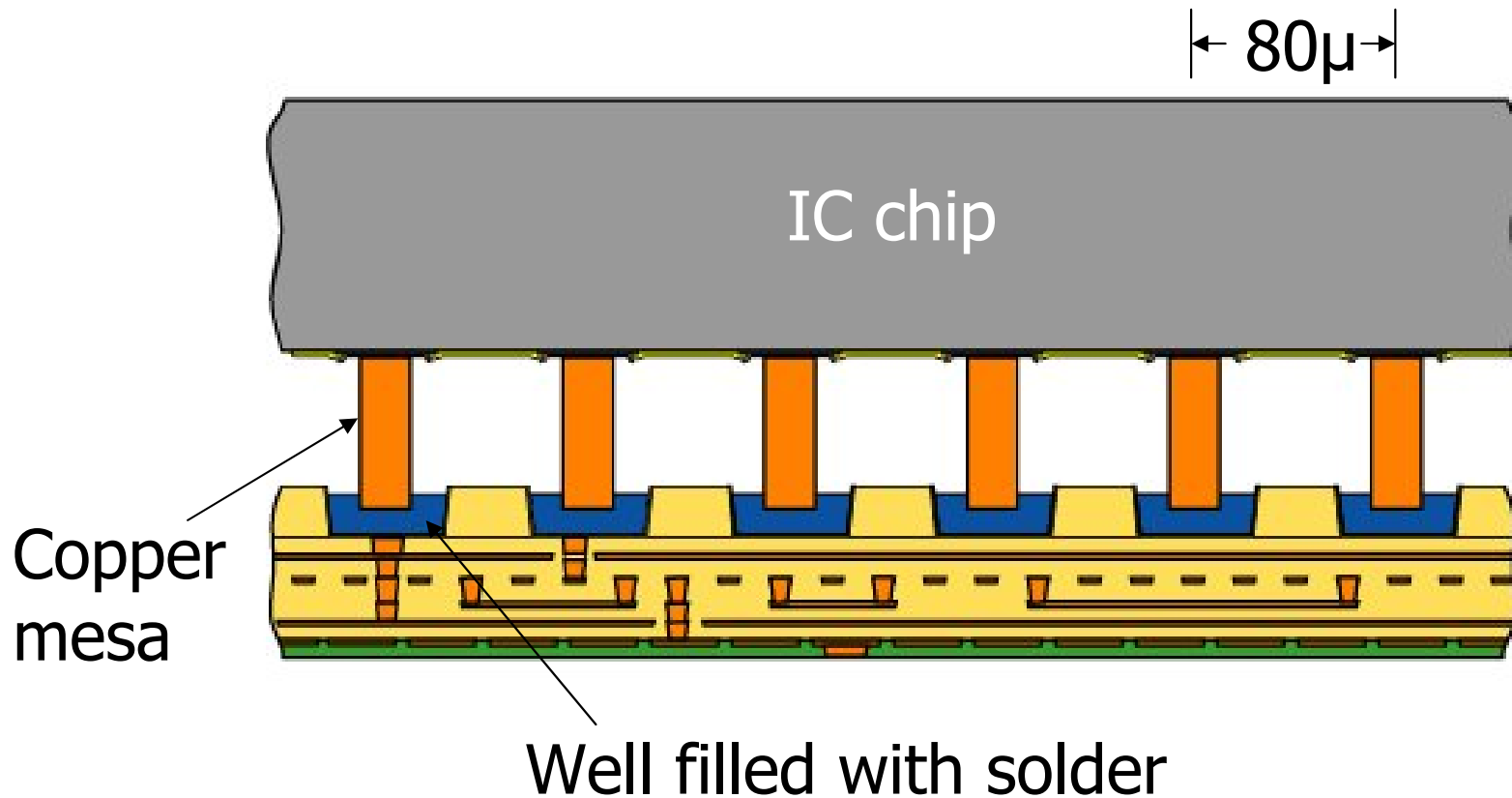
NEW

ITRS requirements for 2010 can potentially be met

- 1) 480W for 310 mm² chip
- 2) 40°C from junction to ambient

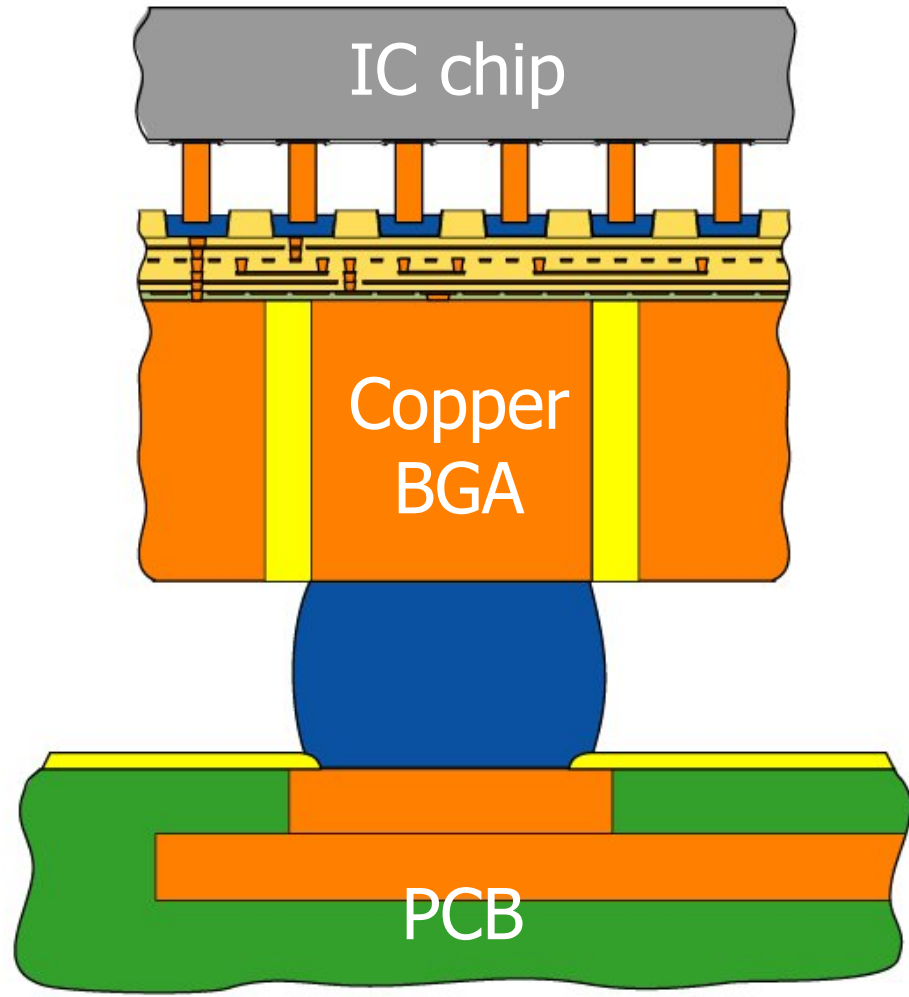


Improved flip chip connection

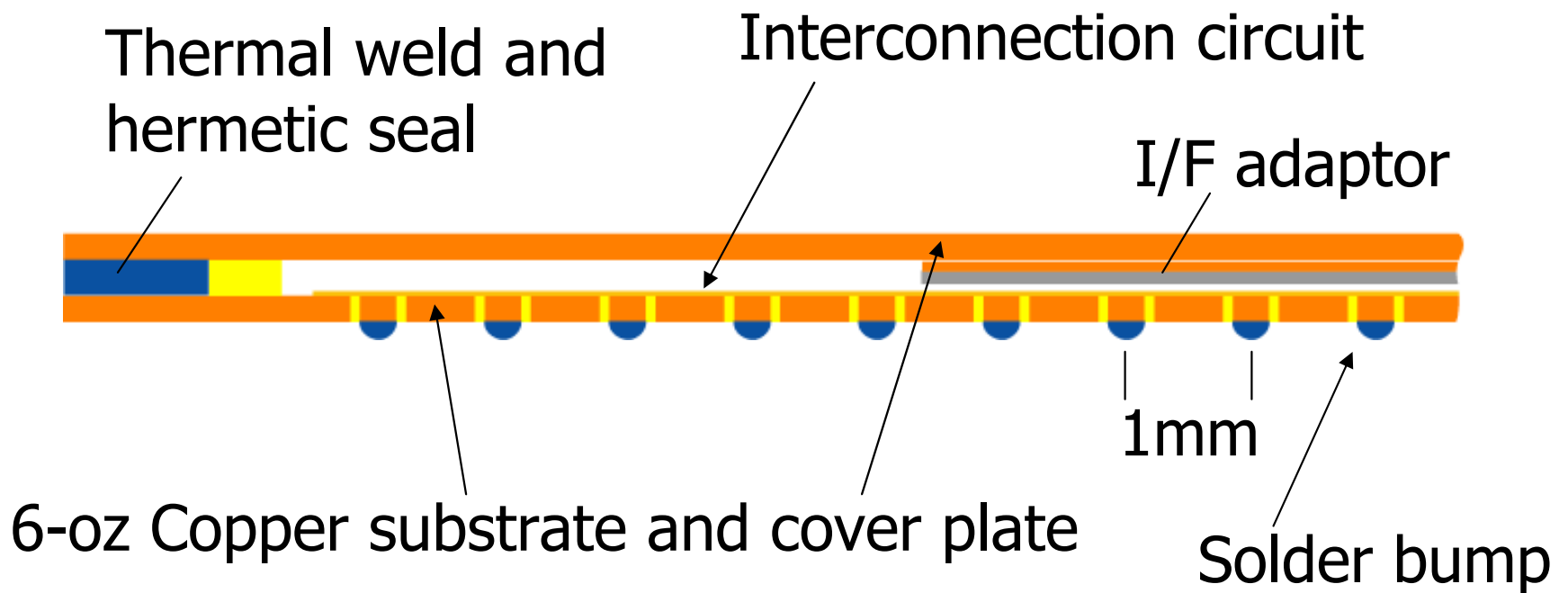


- Good relief of thermally induced stresses
- Deep wells remove criticality of planarity
- Re-workable
- Low force insertion – okay with low-k

Chip-to-board stack-up using copper BGA



Copper BGA



- Notes:
- 1) Hermetic
 - 2) Standard BGA interface to PCB
 - 3) Some radiation protection

Stacked Copper BGA

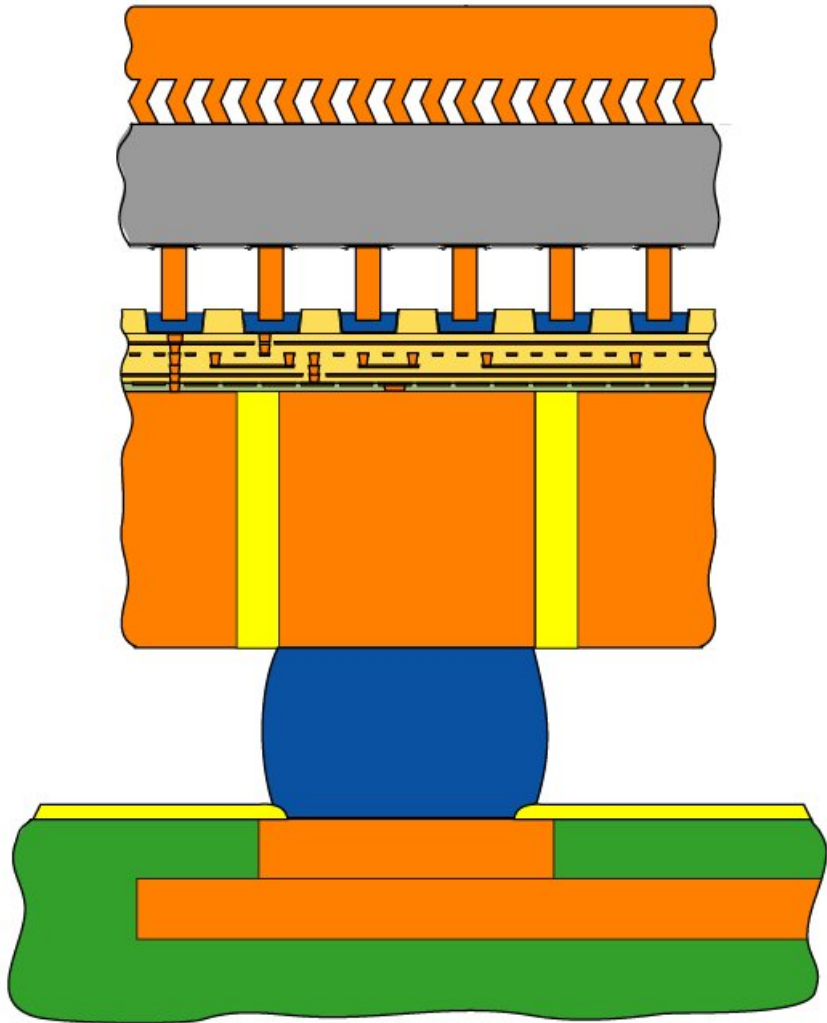


40 mm square area

~ 80 chips

~ 500 watts

Socket for testing known good die



- Fill wells with liquid conductor
 - temporary attachment
- Deep wells make planarity less critical
- Small vertical force
 - okay for low-k dielectrics
- Full speed functional test
 - Really known good die (RKGD)
- $\sim 80\mu$ minimum pad pitch
- Can manage high-power chips
- Adaptable for burn-in



Summary

For 3D packaging:

- Copper solutions take a path between high and low risk
 - Not as risky as wafer-to-wafer bonding but more risky than glass-epoxy
 - Achieve ~ 100X size reduction for a blade server
 - Probably support 10Gbps signaling rate
 - Address heat management problems
 - Address assembly yield problems
 - Available materials and processes – not inherently expensive