Meptec's 4th annual The Heat is On:

High Performance Modules on Copper Substrates

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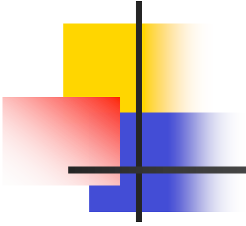
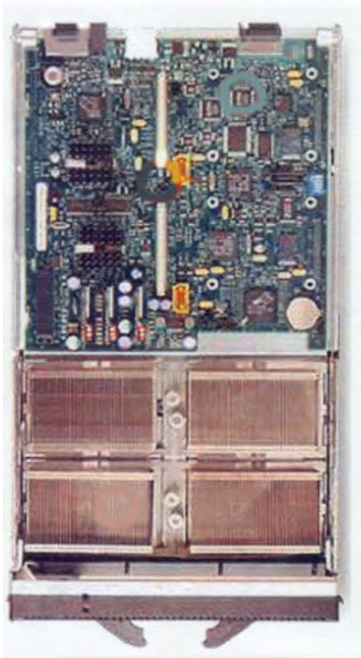
Outline: High Performance Modules on Copper Substrates

- **Copper module perspectives**
  - Size & weight
  - Materials
  - Testing
  - Cooling
  - Manufacturing
- **Construction concepts**
  - Copper substrate with feedthroughs
  - Build up layers
  - Chip attach
  - Wafer level processing & rework
- **Related structures**
  - Semiconductor wafer tester
  - Adaptive heat sink for IC chip
  - Optical fiber interface
  - Alternative repairable semiconductor subsystem (no water)
  - Summary of copper properties
- **Conclusion**

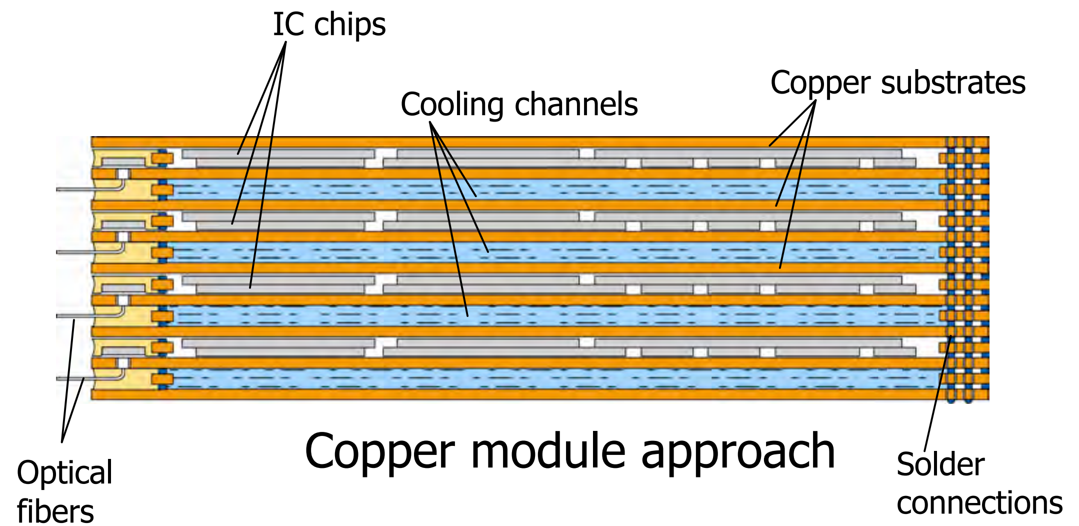


Copper Module Perspectives

Copper Module: Size & weight perspective



Conventional approach

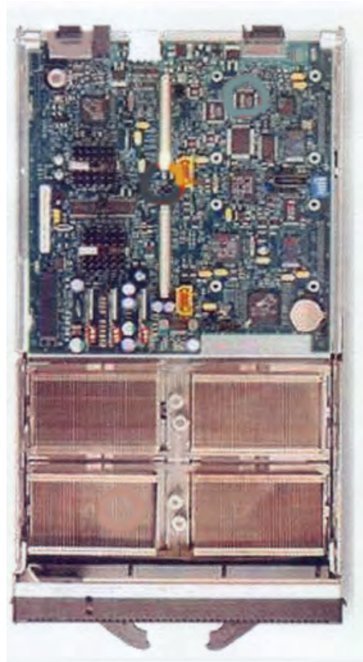


Copper module approach

<5% Size and Weight

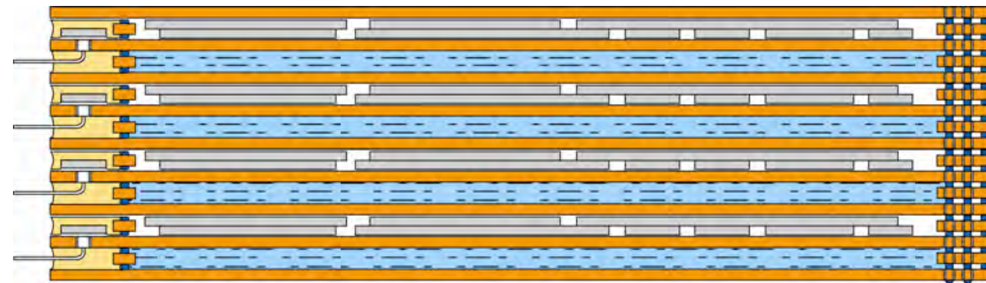
Copper Module: Materials perspective

Conventional approach



Al heat sink	~ 40%
FR4	~ 4%
Silicon	~ 0.1%
Air	~ 55%

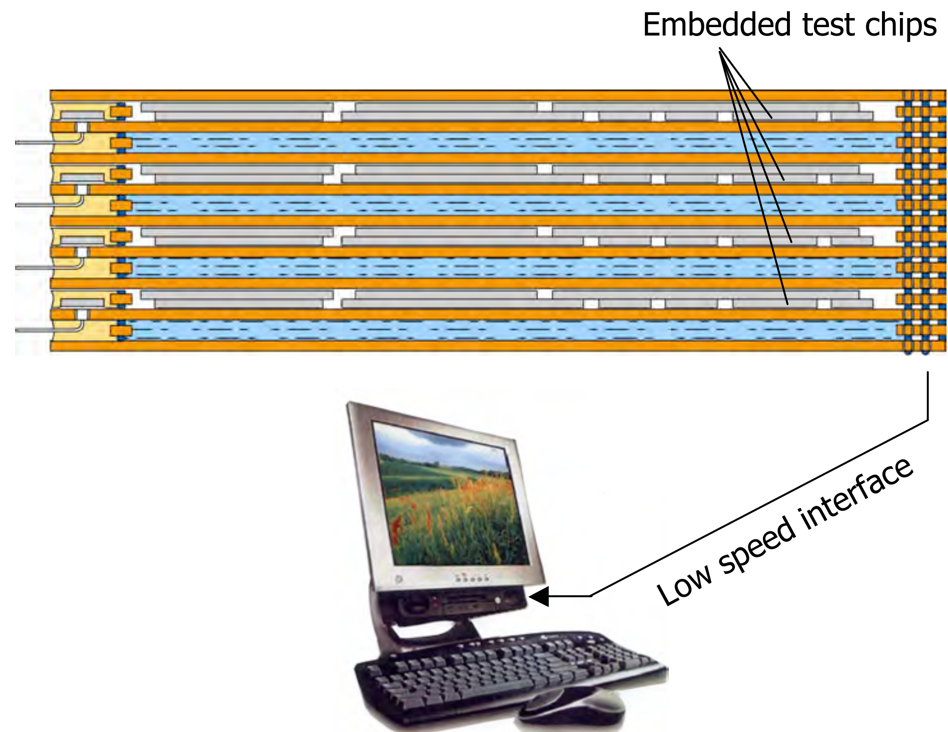
Copper module approach



Copper	~ 40%
Water	~ 35%
Silicon	~ 20%
Air	~ 5%

The work is done in the silicon; the rest is infrastructure

Copper Module: Testing perspective

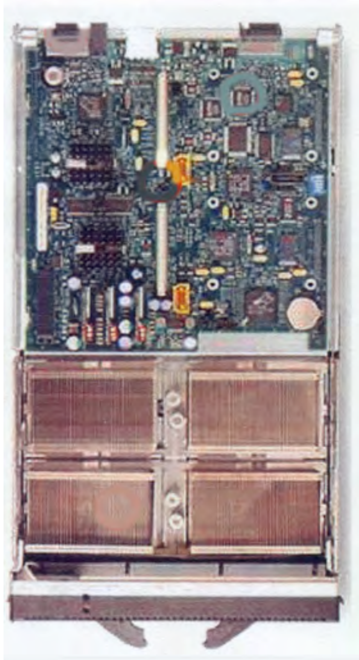


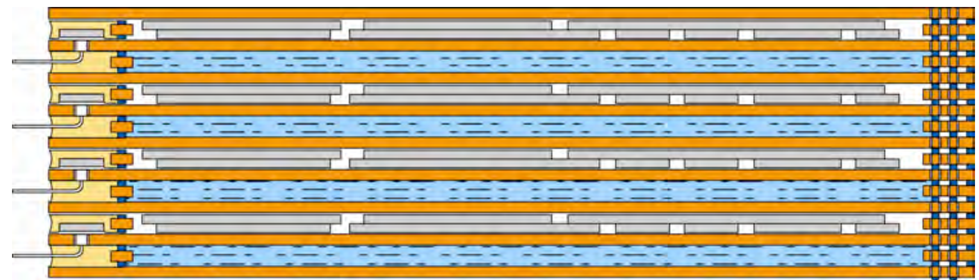
- **Product nodes and tester nodes are far apart**
- **Much of the expense is in the interface**
- **~ $M tester**

- **JTAG + high speed functional test**
- **Sample & compare using system bus**
- **~ $100's computer + ~$5 test chip/module**

The beginning of a test revolution

Copper Module: Cooling perspective





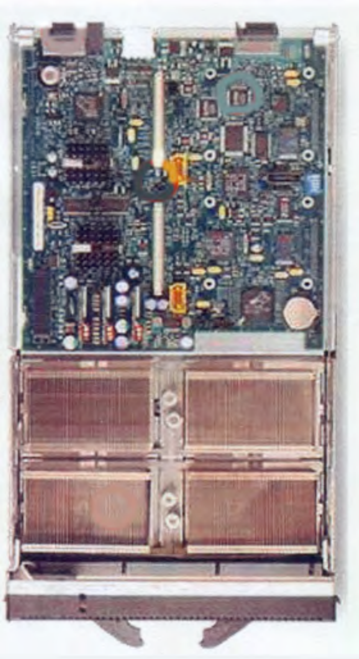
- **Copper is 1600 times more thermally conductive than FR4**
- **Water cooling: ~ 20,000 Watts at 5 liters per minute**

4,000 Watts per liter/min of water

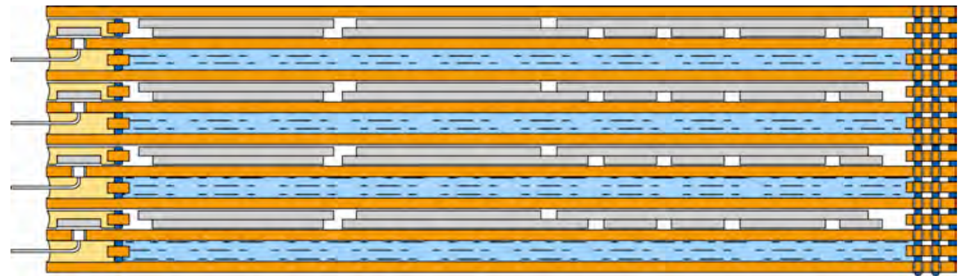
- **PCB substrate is FR4**
- **Air cooling: ~ 2,000 Watts at 325 cfm**
  - 1 cubic foot = 28.3 liters

0.2 Watts per liter/min of air

Copper Module: Manufacturing perspective



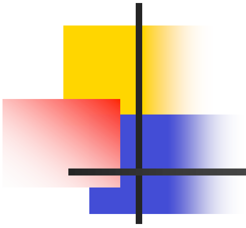
- **4-tier system**
- **Chip → package → board → system**
- **Each package is unique**
  - Custom design constraints
  - Signal integrity issues
  - Power distribution issues
  - Thermal issues
  - Reliability issues
- **Manual test & rework**



- **3-tier system**
- **Chip → module → system**
- **Eliminate conventional packages**
  - Standard design constraints
  - Reliable chip attach (low stress, low shock)
  - More pins for power distribution
  - More test pins
  - Standard thermal environment
- **Automated test & rework**
  - Using embedded test chips

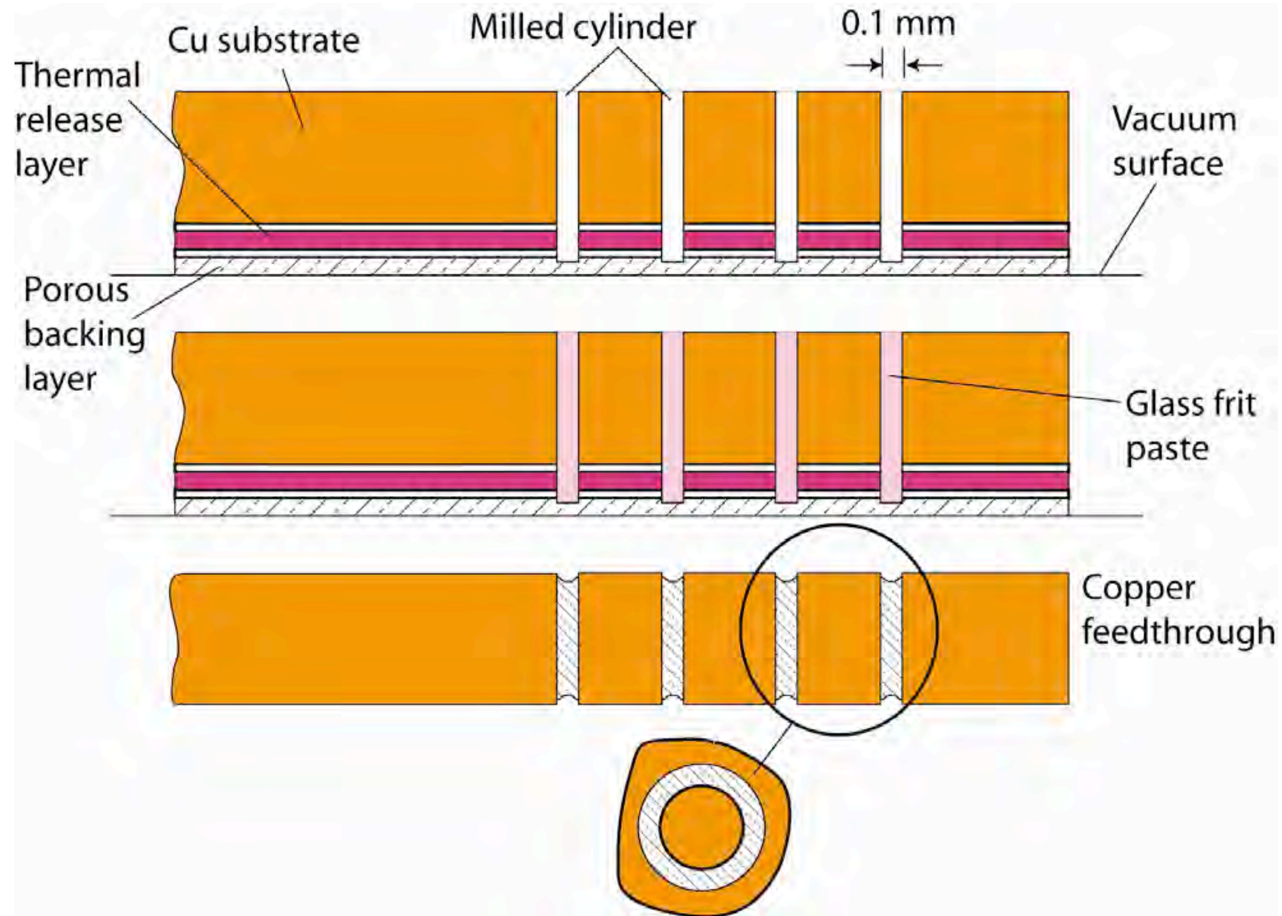
Less material, working harder

More standardization; improved automation potential

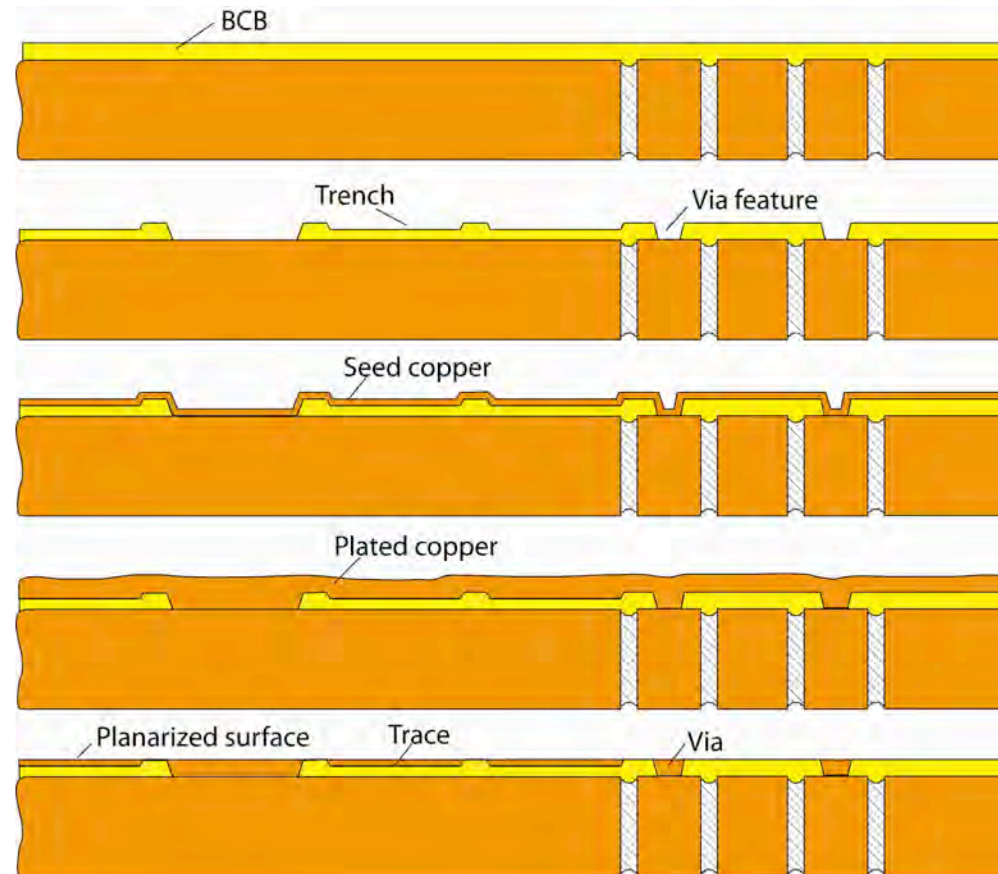


Construction concepts

Construction: Copper substrate with feedthroughs

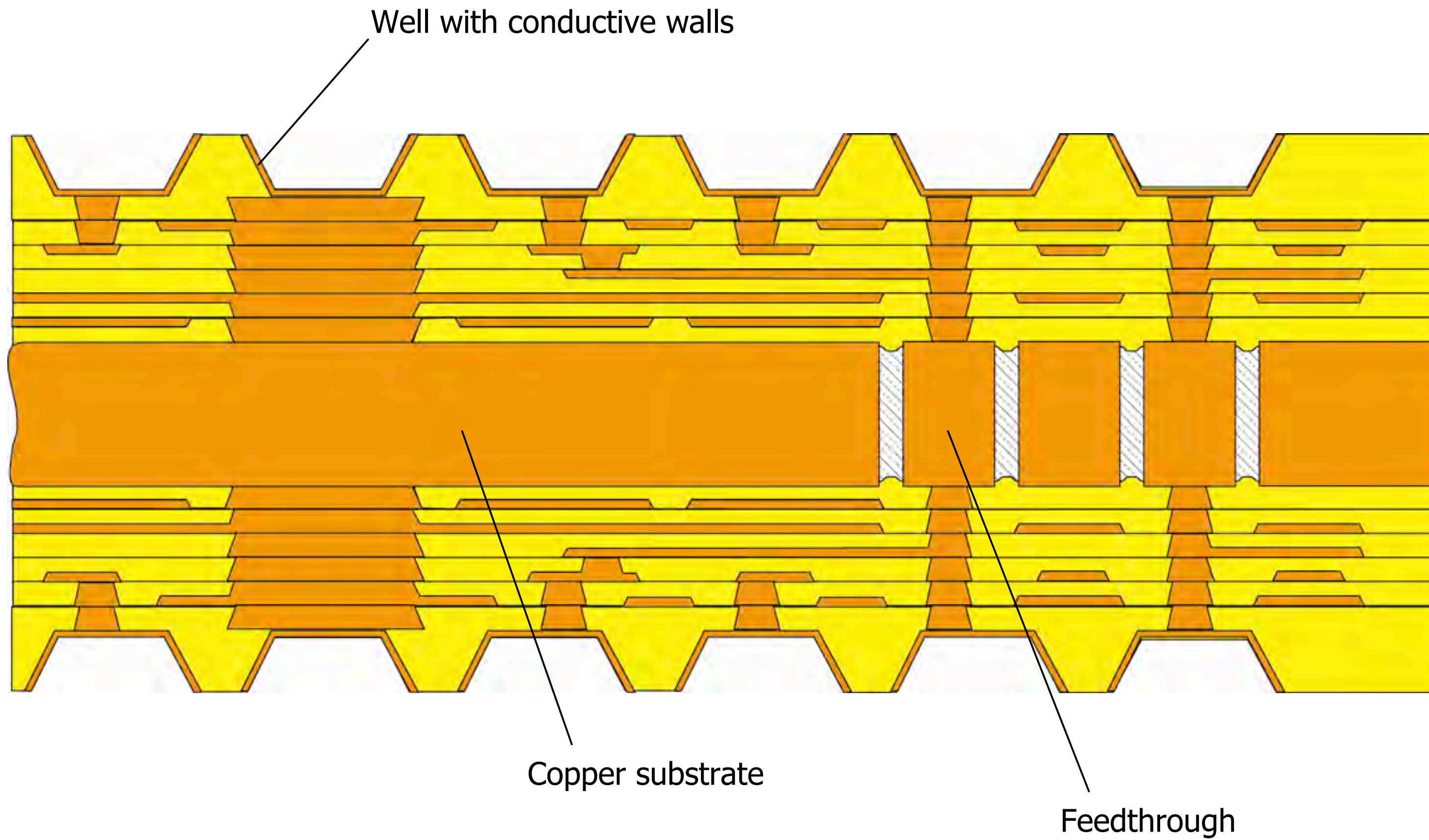


Construction: Build-up layers - I



Treat the copper substrate like a semiconductor wafer or a flat glass panel

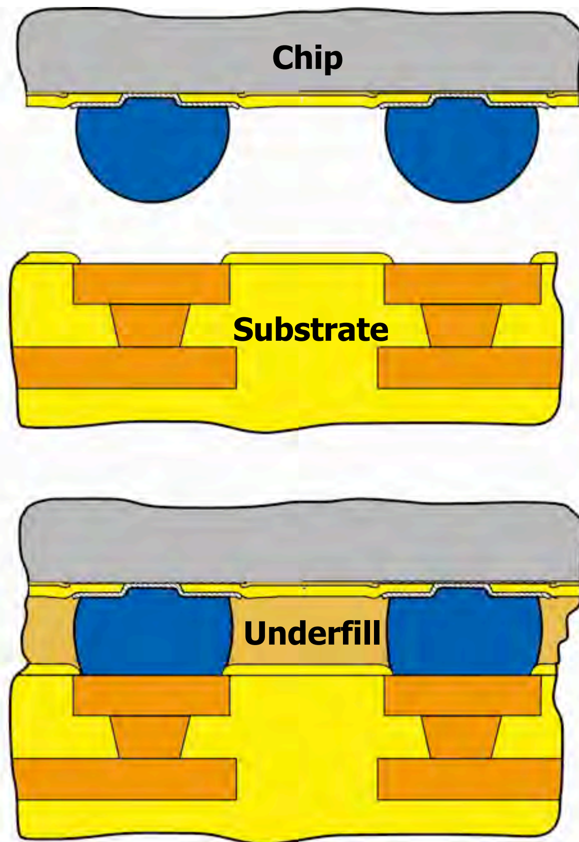
Construction: Build-up layers - II



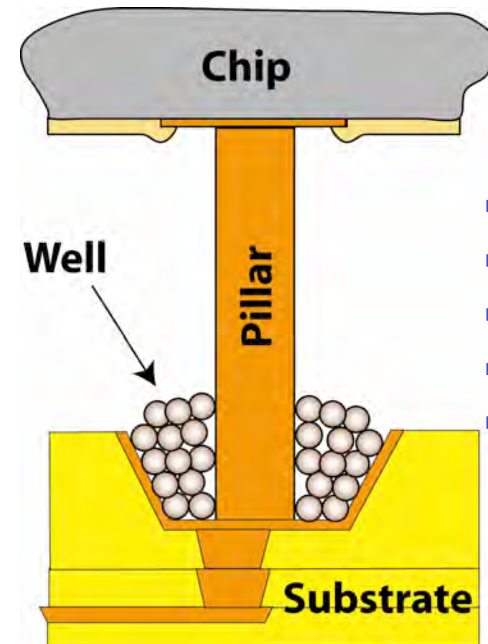
Copper provides support, controlled impedance capability, shielding, and excellent heat conduction

Construction: Chip attach

- Mature
- Coarse pitch
- Not Reworkable (>3mm chips)



C4 BGA

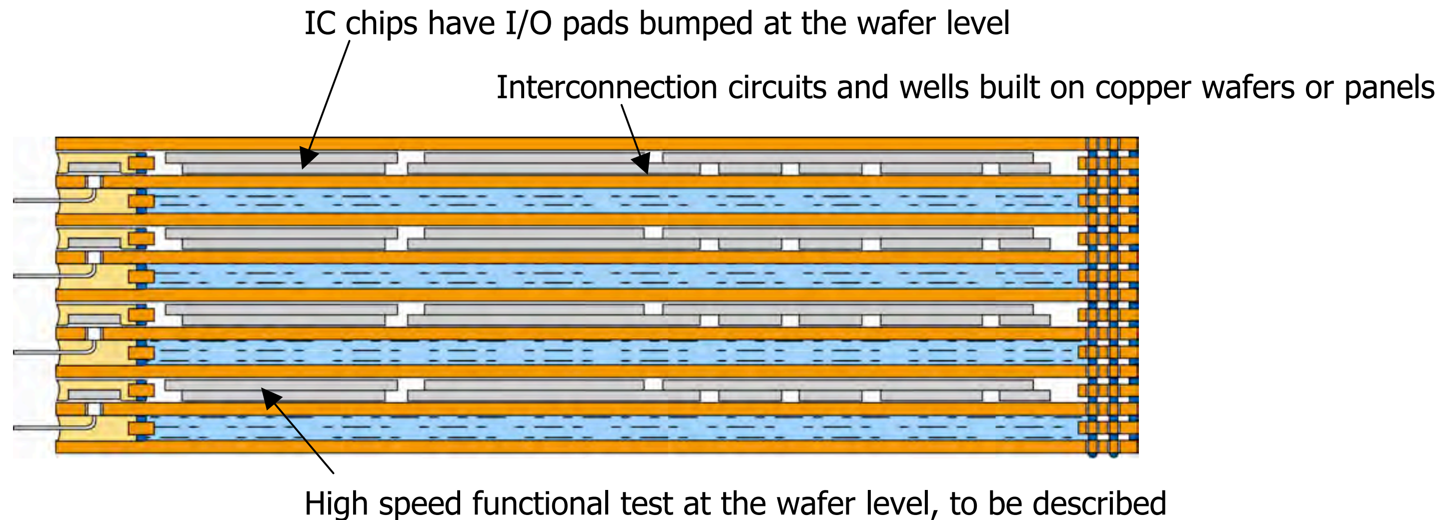


Pillar-In-Well

- Flexible
- Adaptive
- Fine pitch
- Wafer level
- Reworkable

Select from old or new flip chip attachment methods

Construction: Wafer level processing & Rework



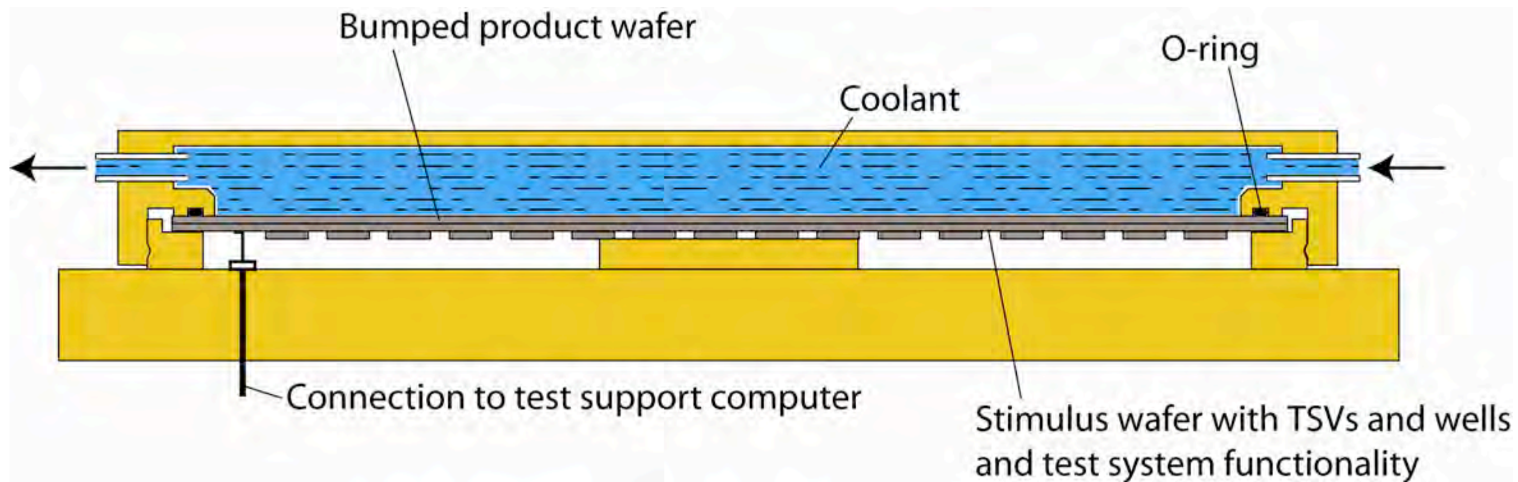
- **Wafer level processing and new test method enable automation**
  - Especially an integrated process for [Assembly + Rework]
- **Rework is achievable at all integration levels: both module & system**
  - Some chips also support reworkability, e.g., memories having redundant circuits
- **Copper circuits can be fabricated like semiconductor wafers or glass panels**

Rework is the forgotten stepchild of system integration

System designers know about it, but don't talk about it much,
perhaps because the current level of capability is embarrassing

Related structures

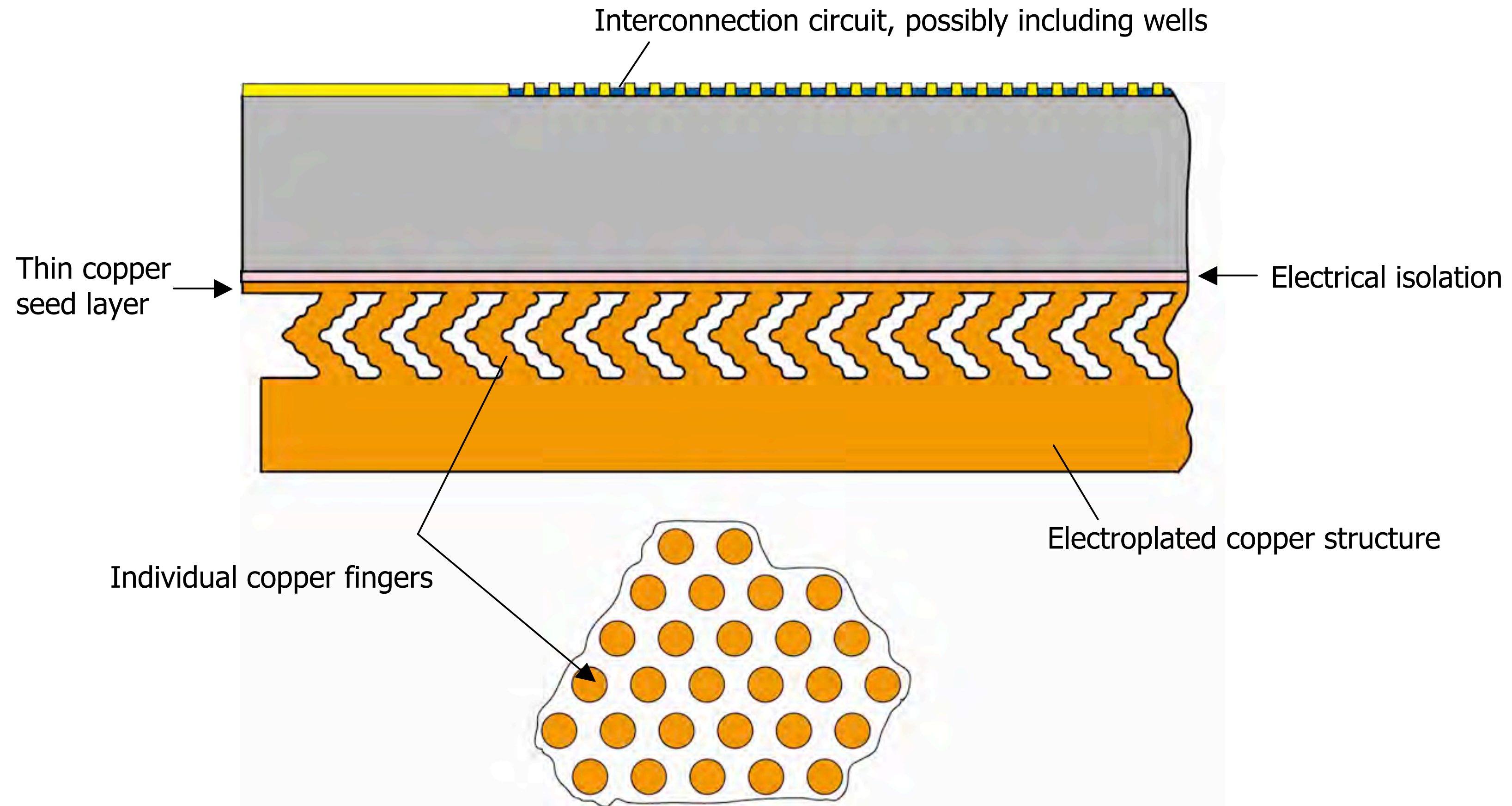
Semiconductor wafer tester



- **~ 20,000 watts of cooling at 5 liters/minute**
- **~ 350,000 simultaneous probes on the wafer**
  - Near zero insertion force using a liquid conductor in the wells
- **Functional test at ~ 10 Gbps**
  - Full speed and full power and maximum parallelism

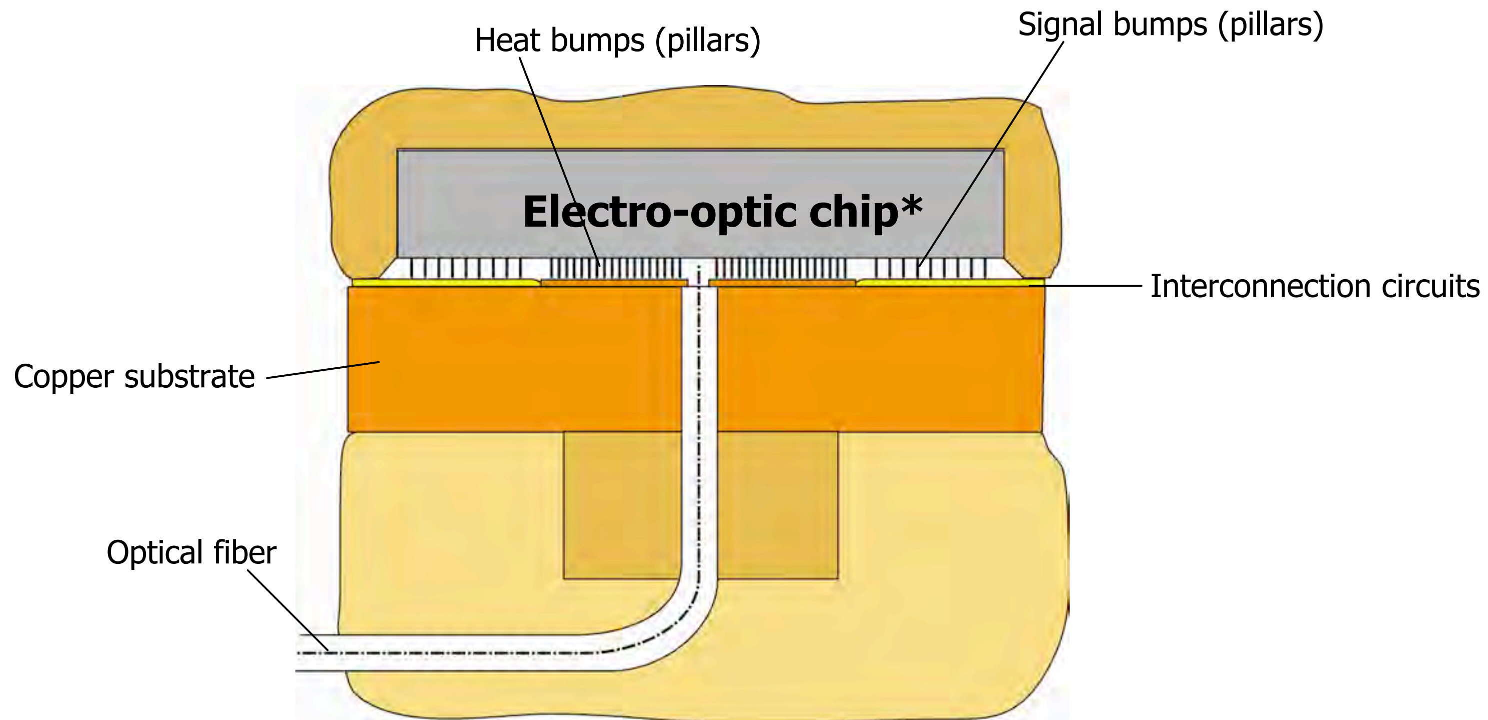
Capability exists to build this tester today

Adaptive heat sink for IC chip (or silicon integration platform)



Wafer level packaging implementations on both sides of the IC wafer/chip

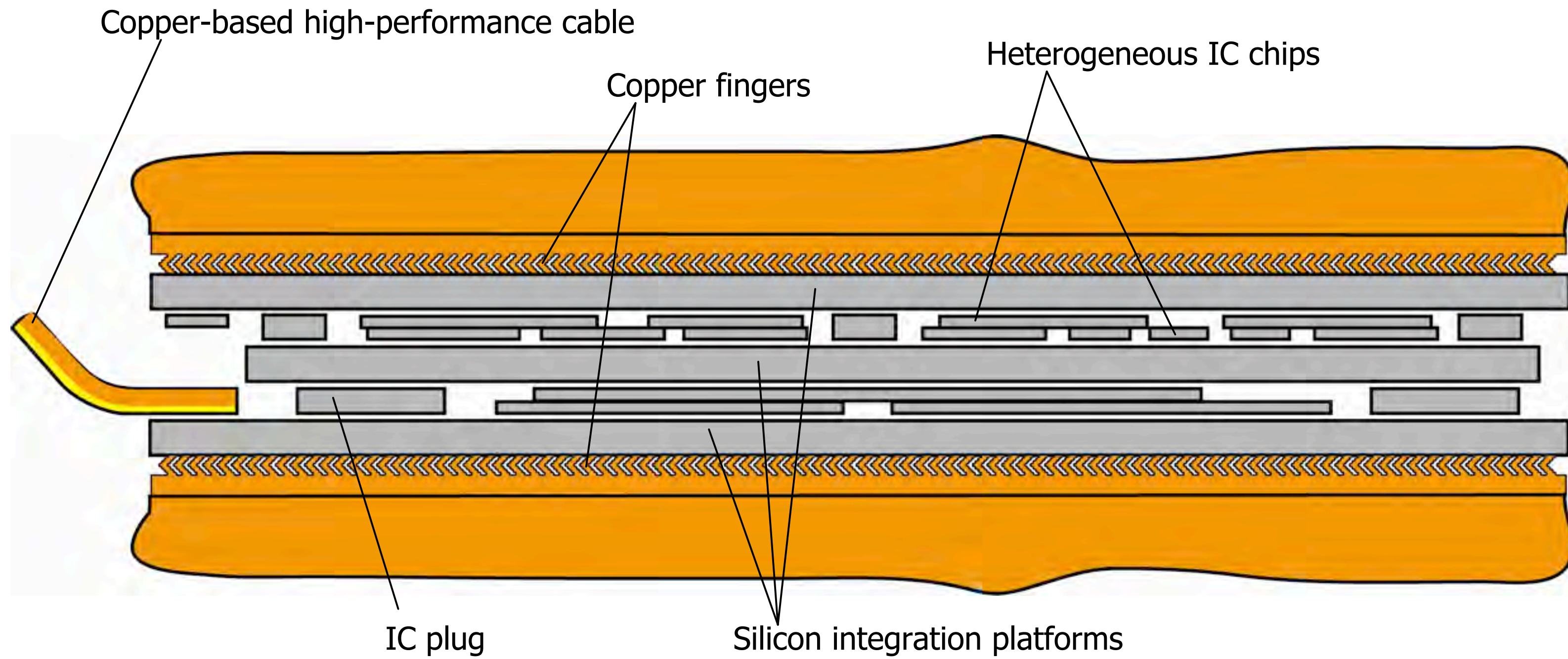
Optical fiber interface



* Hypothetical chip, may not be realizable ………. yet

Package design anticipation

Alternative repairable semiconductor subsystem (no water)



Minimal air: maximal function

Summary of copper properties

- **Available and inexpensive in multiple thicknesses and types**
  - e.g., Increased stiffness using dispersion strengthened copper
- **Good mechanical support**
- **Provides electrical ground plane**
  - Transmission line structures
  - Minimize EMI via electrical screening
- **Excellent thermal conductor, much better than alternatives**
- **Impervious to water**
- **Manufacturable like a semiconductor wafer or flat panel**

Conclusion

- We cannot continue to rely on Moore's Law to bail us out of power problems. In the coming technology nodes, we will have to choose between high performance and low power*. For products like servers that need high performance, continued improvement must come from system elements other than the silicon. This is why new integration concepts like those discussed today have become necessary, not just "nice to have".
- It is not enough to solve the issues one at a time. There needs to be a *simultaneous* solution to power, density, testing, and low cost production. This will likely be a "system level" solution.
- * See for example, the ISSCC keynote by Mike Muller, CTO of ARM.