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Copper Pillar Well Methodology and Implementation in a VLP FB DIMM

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Owner

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2006 KGD Packaging
& Test Workshop
Sept. 10-13, 2006
Napa, California

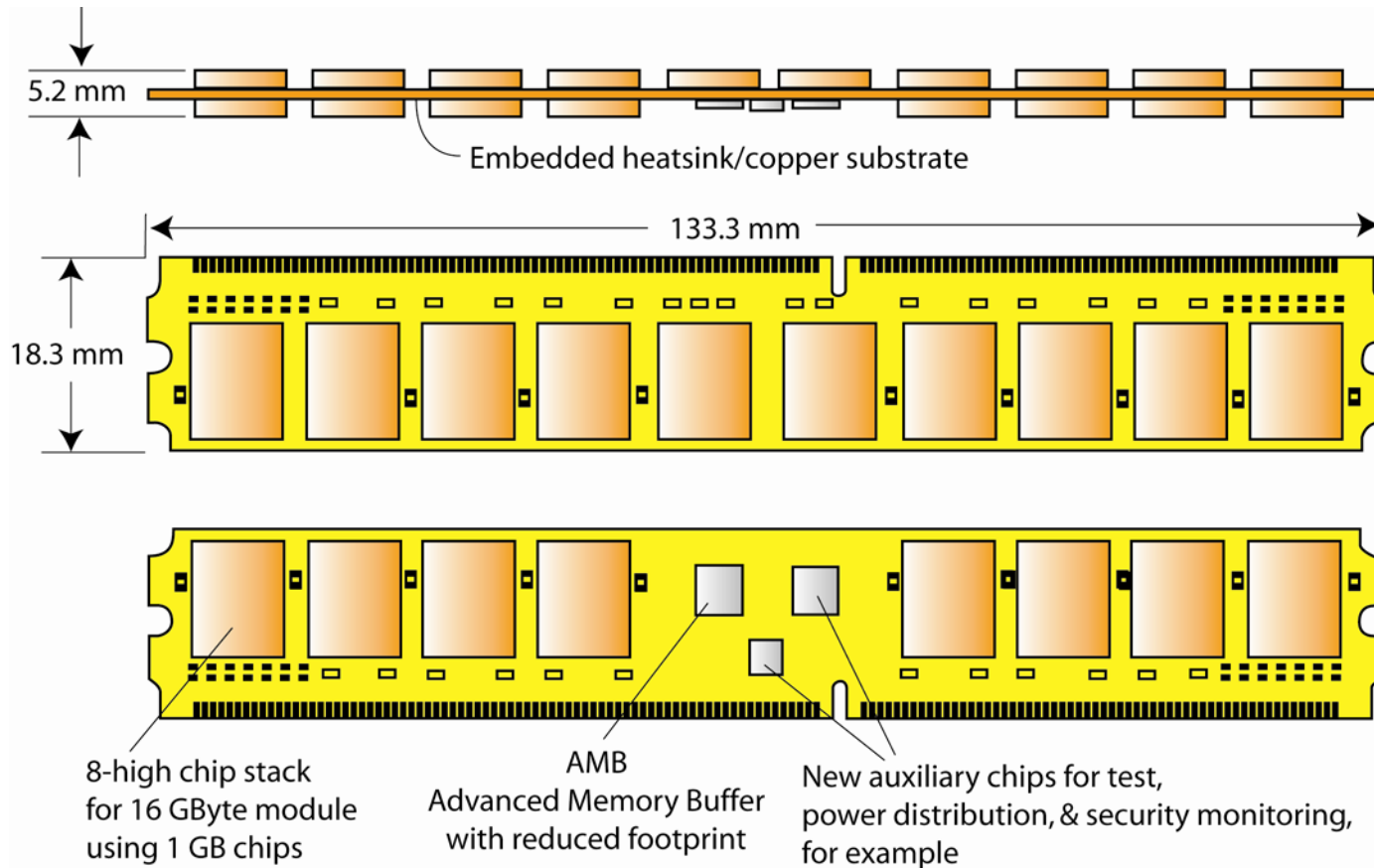
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Outline

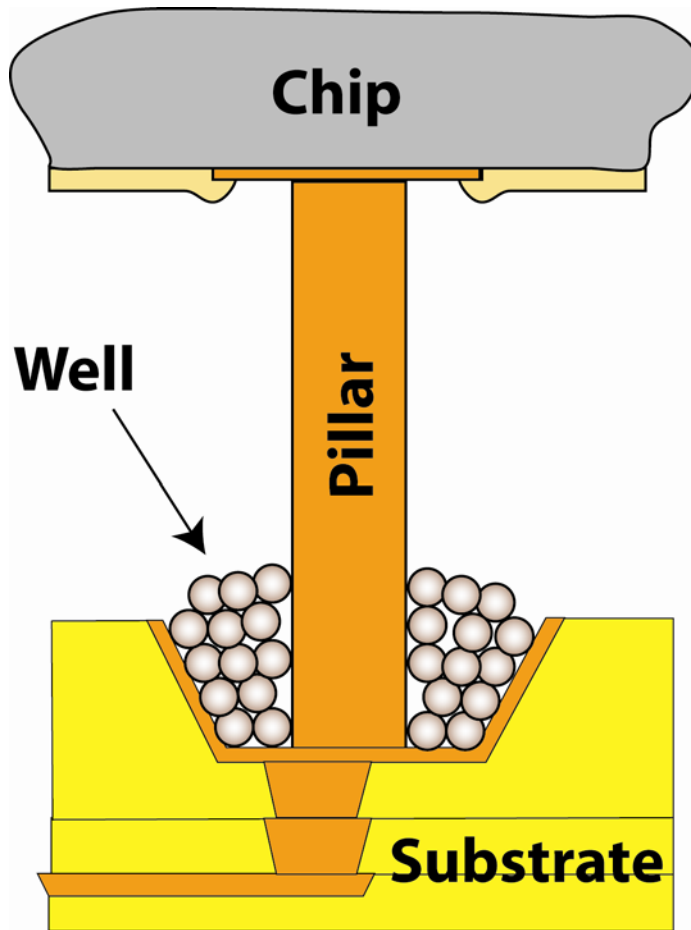
- Conceptual design of memory module
- Copper-pillar-well (CPW) connector
- Copper pillar fabrication
- Substrate fabrication
- Assembly/test/rework
- Panel form factors
- Extensions to non-memory applications
- Summary of future possibilities

Conceptual design of memory module*



* VLP FB DIMM = Very Low Profile Fully Buffered Dual In-line Memory Module

Copper-pillar-well (CPW) connector



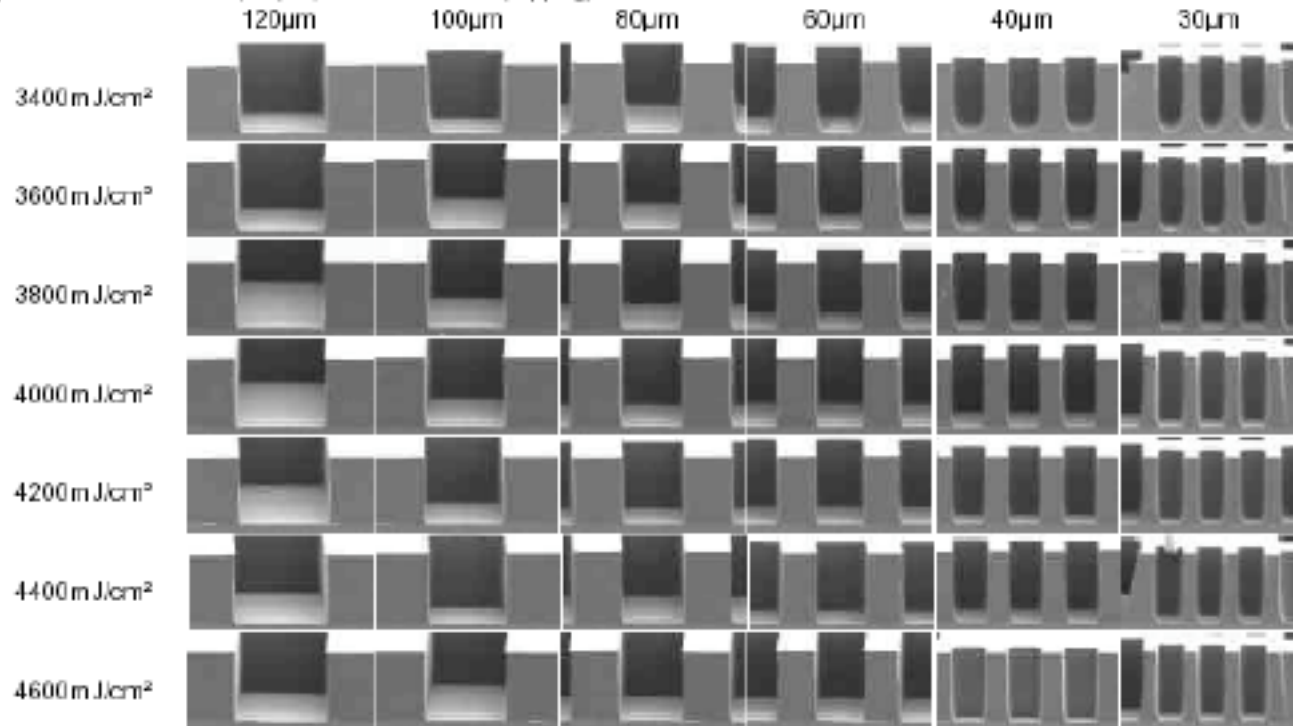
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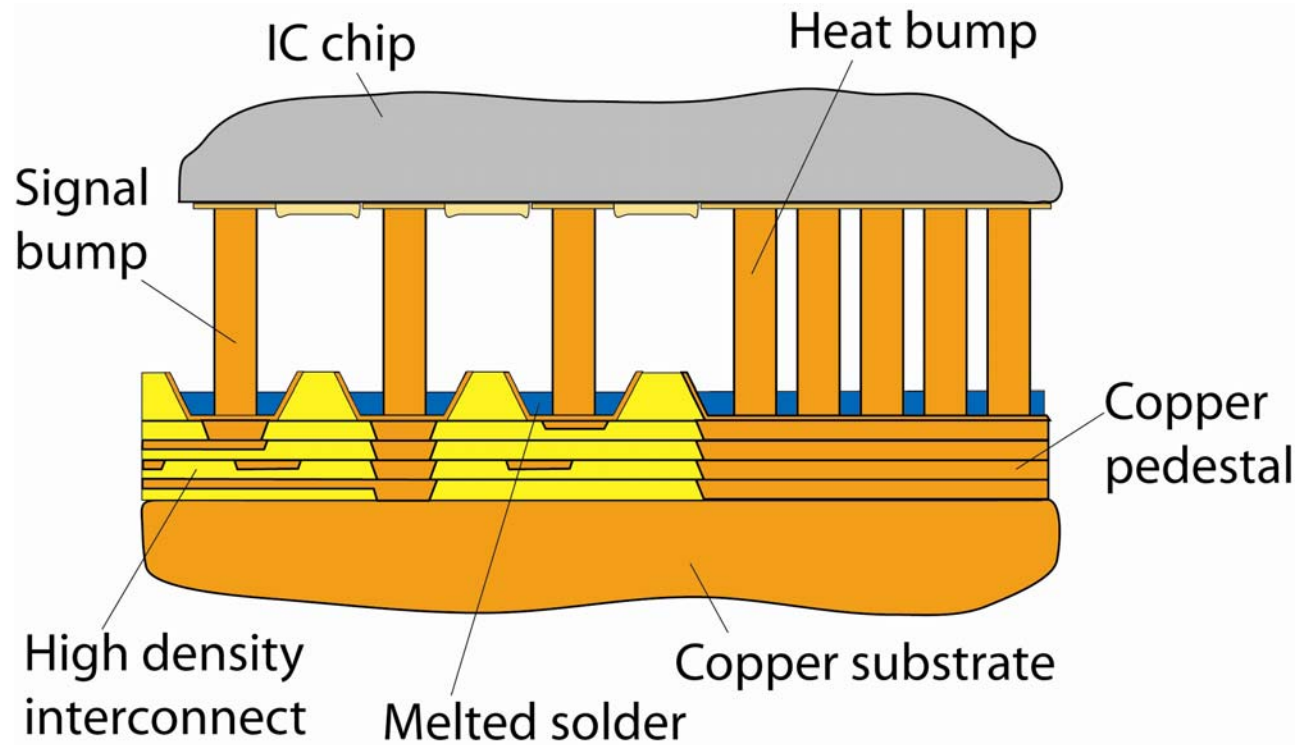
Copper pillar fabrication(1) - Resist

Substrate: 6inch Cu(2000Å) on Ti(500Å) on Si, Film Thickness: 110µm
Pre Bake: 105°Cx250sec>>115°Cx500sec(HP) Focus Latitude: -40µm
Exposure: UltraTech Stepper Saturn-Spectrum-3 (g,h-line)
Development: AZ 300H Developer(1:5) 23°Cx4min30sec(Dipping)



- Clariant AZ Exp 100XT
- Experimental resist
- Not a slam dunk
- 5:1 aspect ratio

Copper pillar fabrication(2) – signal bumps & heat bumps

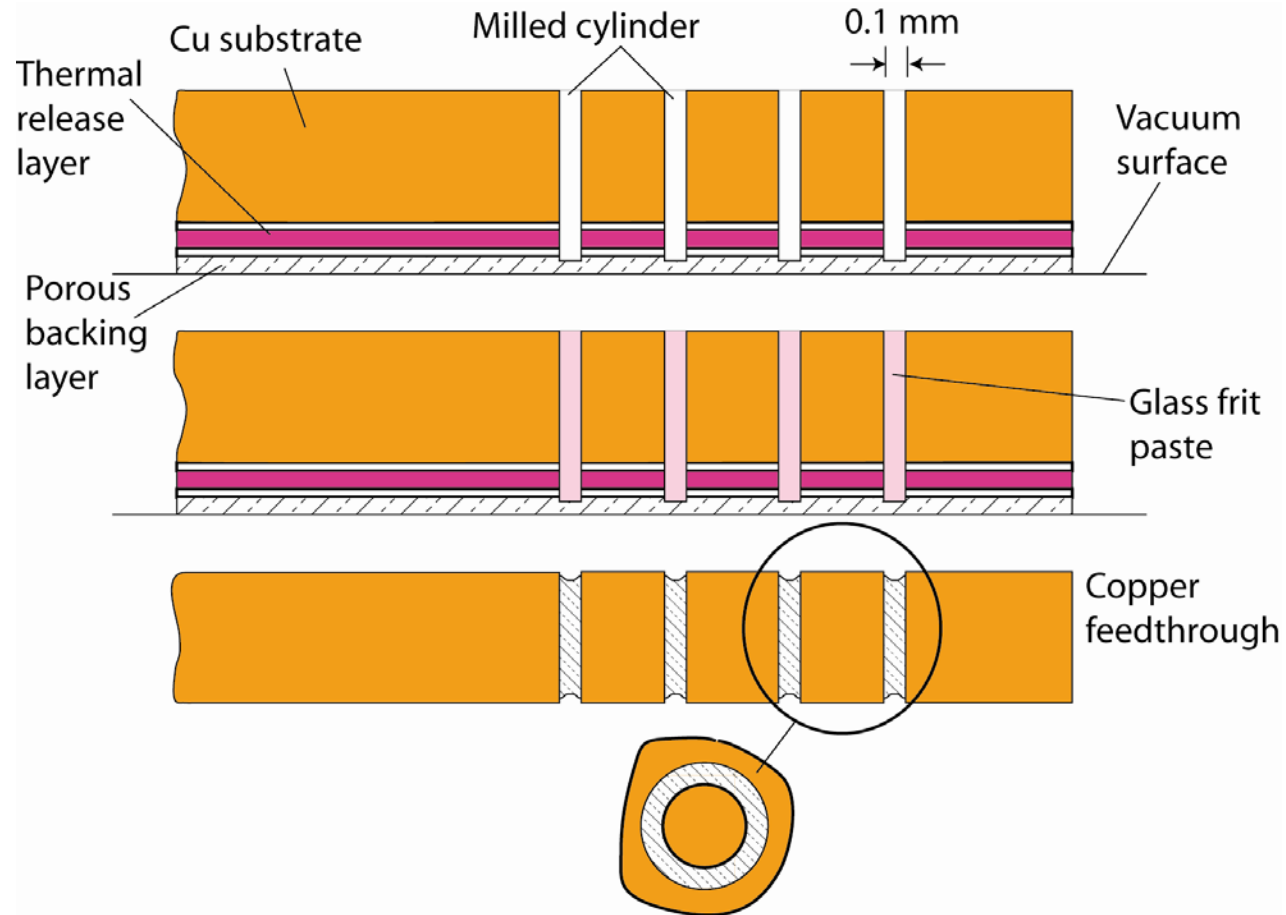


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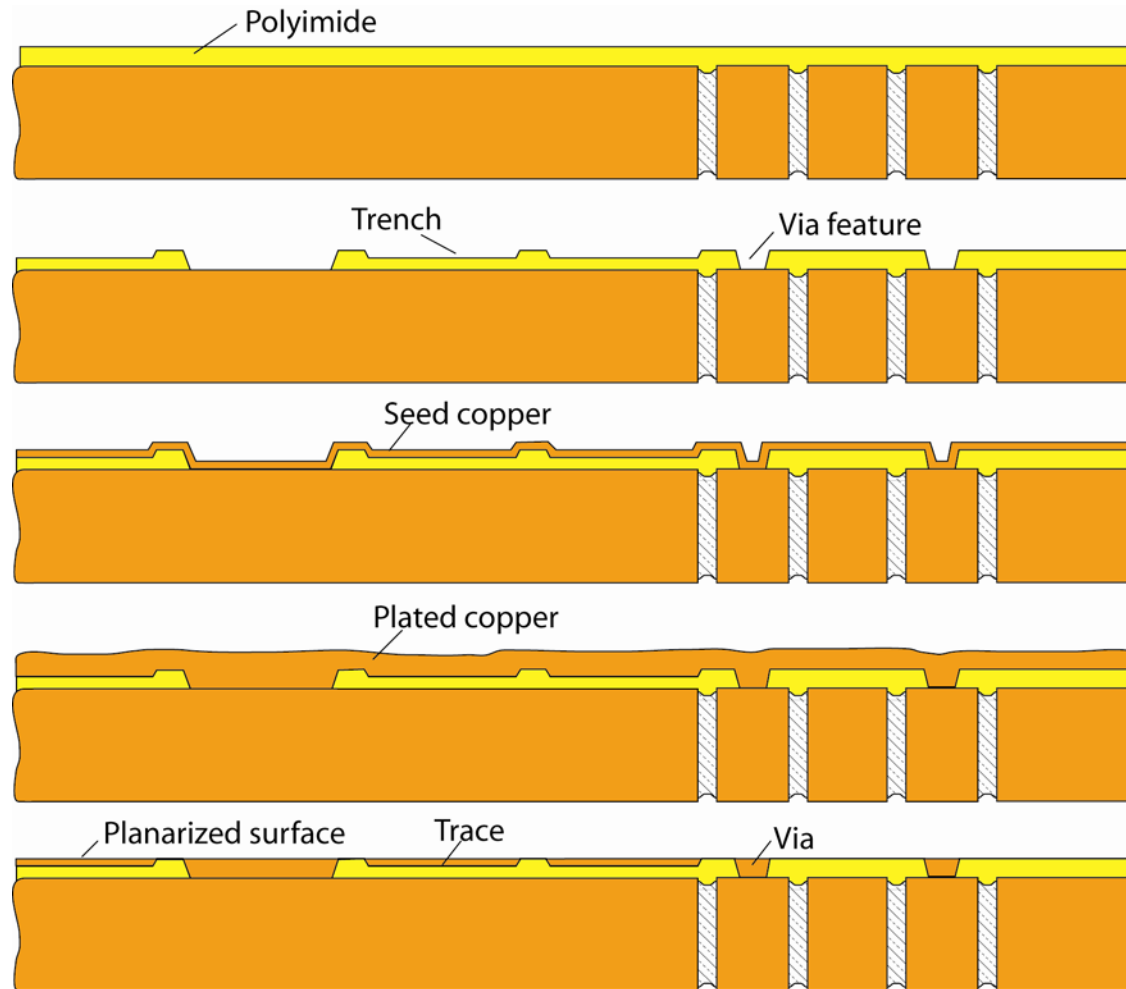
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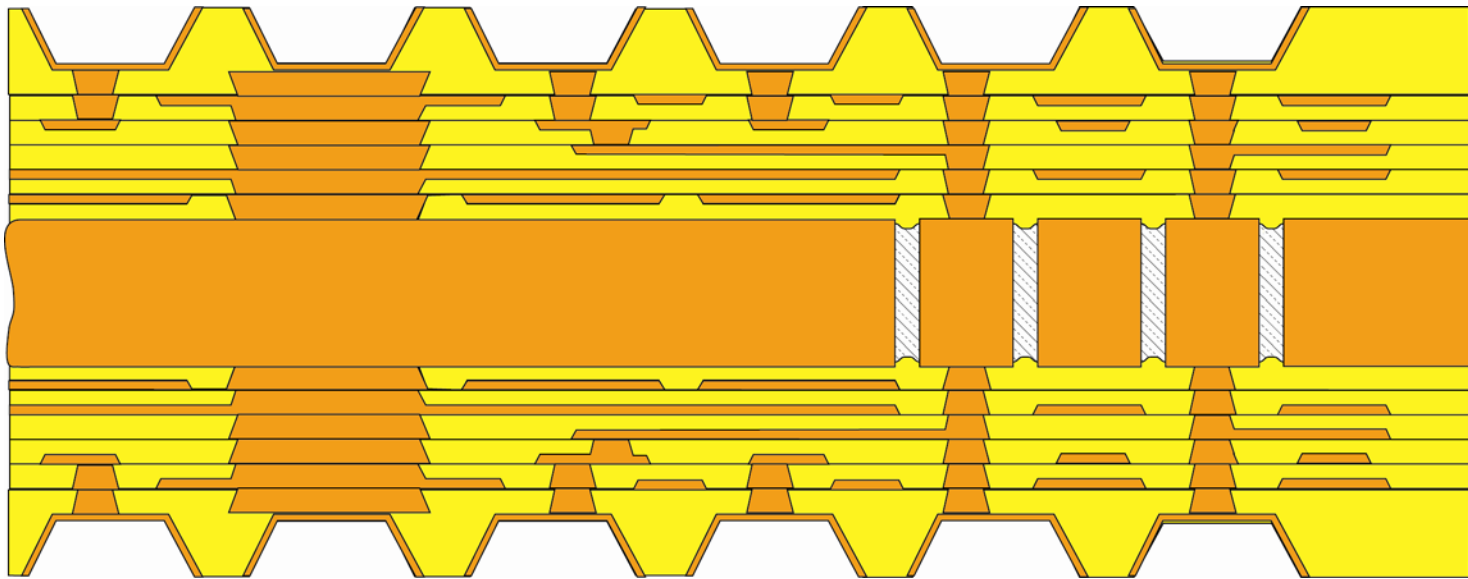
Copper substrate fabrication (1)



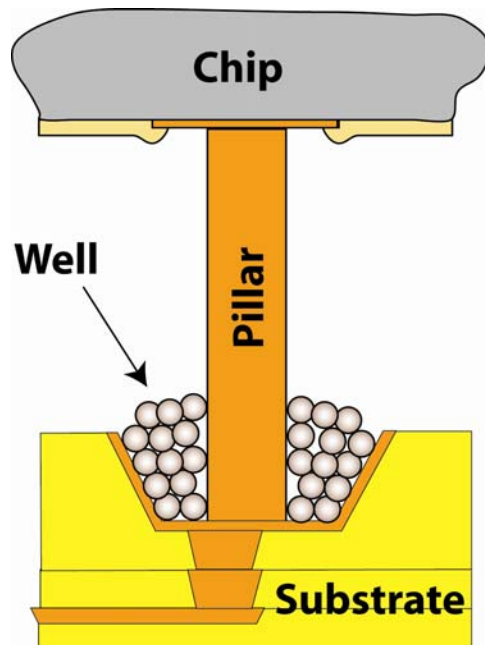
Copper substrate fabrication (2)



Copper substrate fabrication (3)



Assembly/Test/Rework (1) - Summary

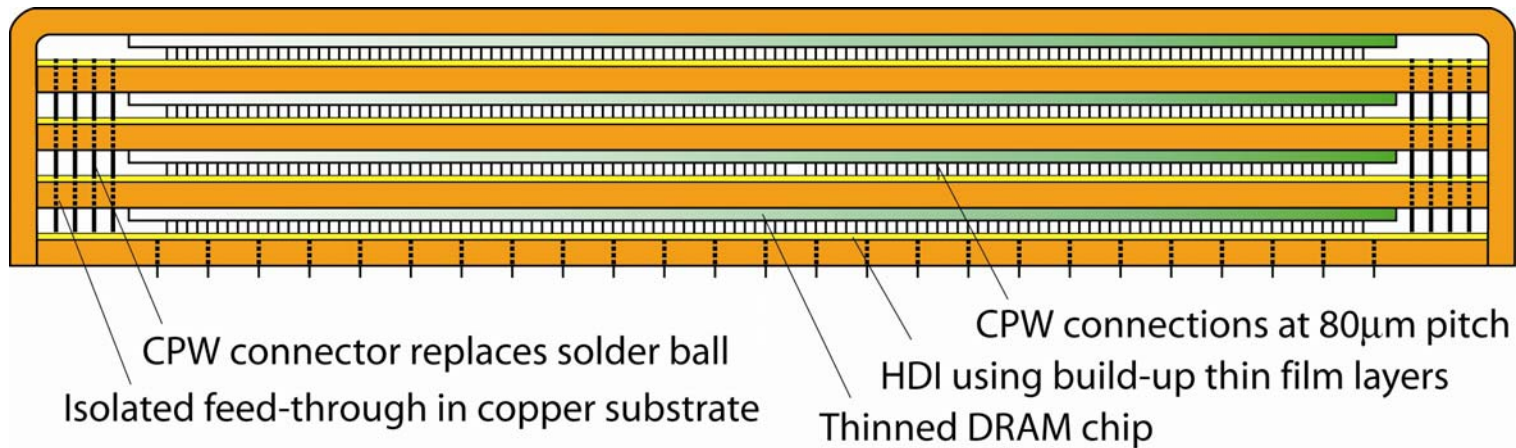


- Bump semiconductor wafer
- Fabricate substrate with wells
- Prepare 80Au20Sn particles
- Fill wells with particles
- Align chip with substrate
- Place bumps on wells
- Urge bumps into wells (ultrasonic)
- Test using local test chip
- Rework as required
- Continue 3D assembly
- Melt solder

Assembly/Test/Rework (2)

– Stacked assembly

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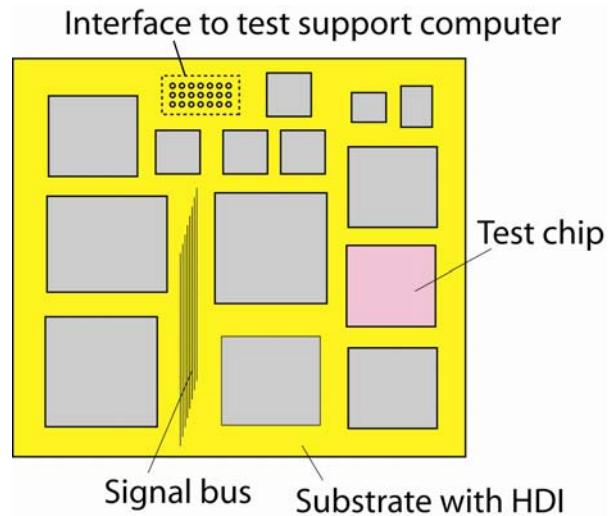
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Assembly/Test/Rework (3)

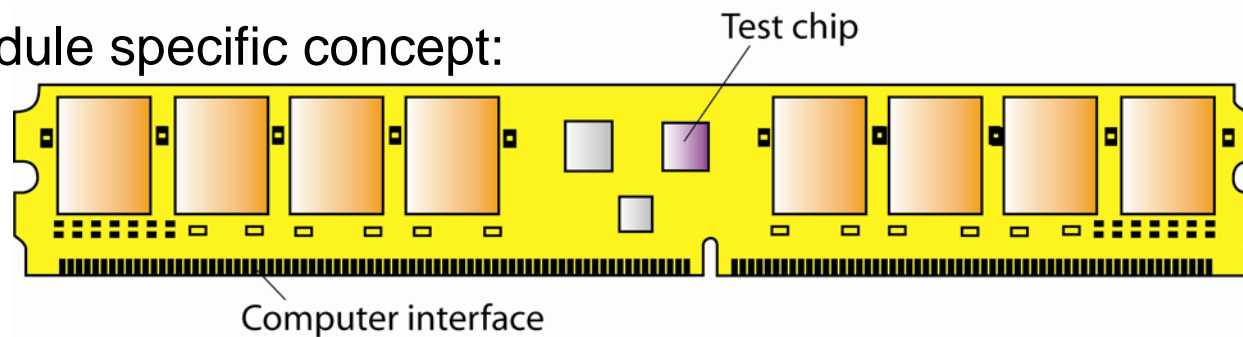
– New test concept

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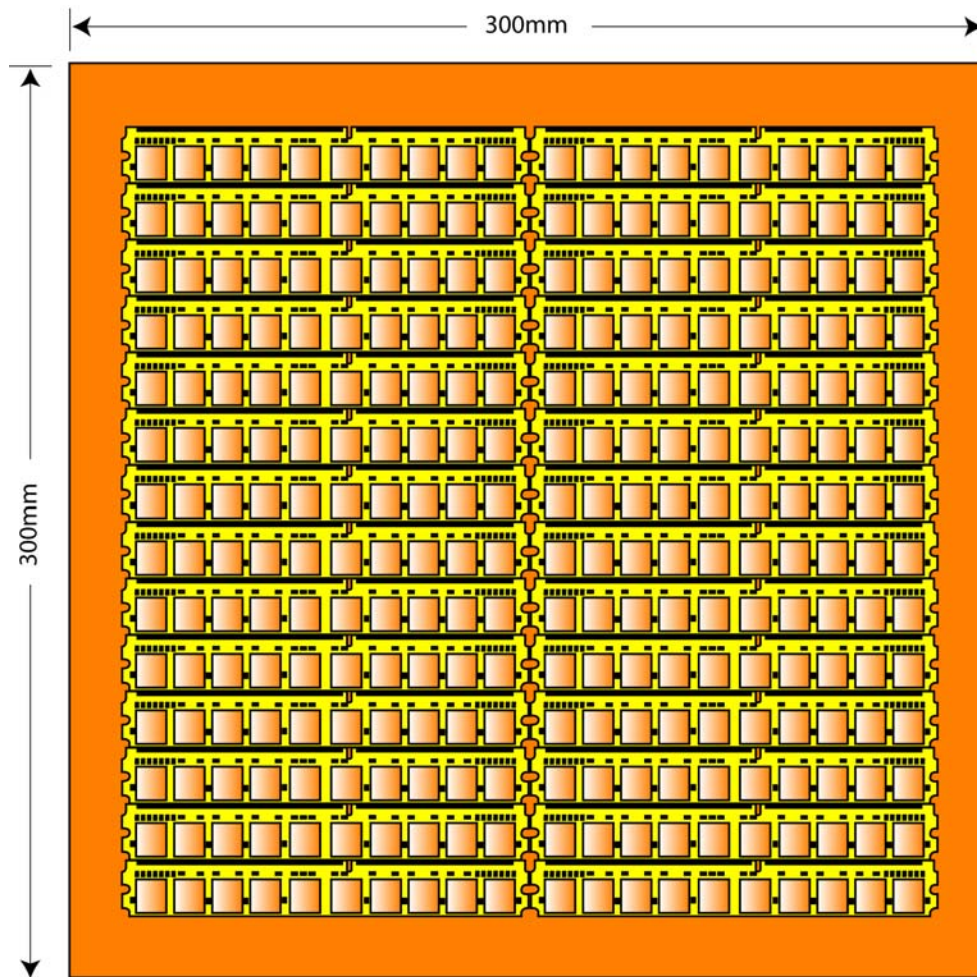
General concept:



Module specific concept:

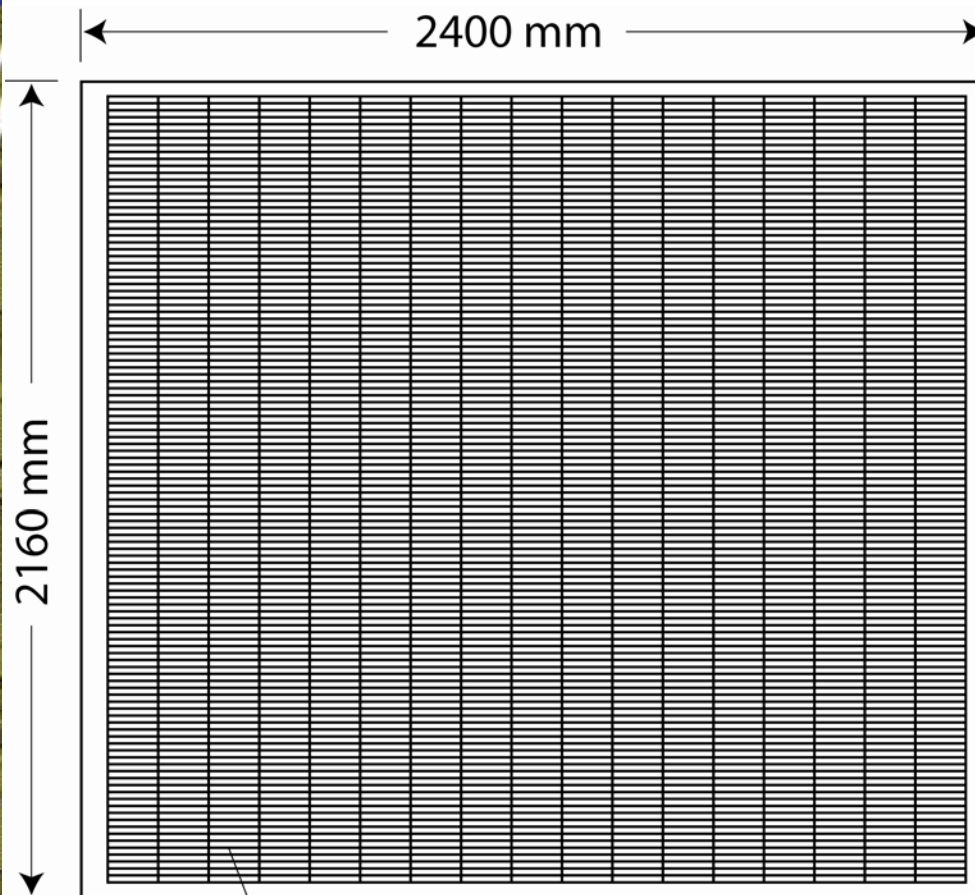


Panel form factor (1)



300 x 300 mm panel
28 modules per panel
4032 die per panel
100% assembly yield

Panel form factor (2)

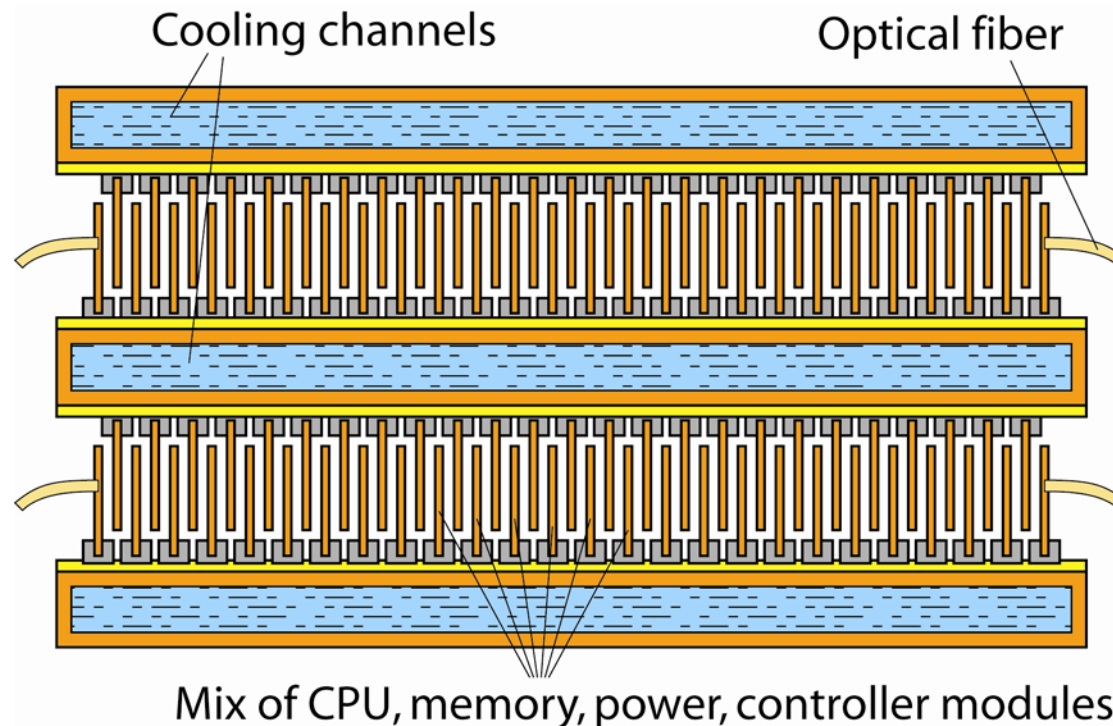


16-GByte VLP FB DIMM modules

Flat panel display
AMLCD process
Generation 8
~ 8ft x 7ft panel
0.8 μm features
6 mask layers
\$15 per diag. inch
\$2,000 per panel

Adapt to foil on glass
1955 modules/panel
8 layer stack, ea. side
~ \$25 subst cost/DIMM
281,000 die
100% assy yield

Using standard DIMMs in non-memory applications- supercomputer concept



Well-tested, repairable, & adequately cooled



Summary of future possibilities

- High performance substrates
 - Support the highest performance IC chips
 - Support new levels of power density
 - Technology path to medium cost using 300mm panels
 - Path to low cost using FPD panels
- New CPW flip chip connector
 - Enables arbitrarily complex 3D assemblies that are well-tested, adequately cooled, and repairable
 - 100X size reduction is possible (e.g., for a server)
 - 100% assembly yield is achievable
- VLP FB DIMM
 - Very low profile is achievable
 - 16 GByte modules are possible in 2007
 - Low cost is achievable if investments are made