Chip on flex with 5-micron features

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ABSTRACT

A new module packaging method is proposed for electronic systems comprising a motherboard and integrated circuit (IC) chips. Pitches of 10 microns for conductive traces, and 100 microns for bonding pads are achievable. The enabling technology is glass panel manufacture, using equipment and techniques similar to those employed for fabricating liquid crystal display (LCD) panels. Flexible circuits are produced on a glass carrier using a release layer, and the carrier is removed after most of the processing is complete. IC chips are stud bumped and flip chip bonded to wells filled with solder, provided on the flexible circuit. The fabrication density achievable with wafer level packaging (WLP) using silicon wafers is substantially more than is needed for module packaging, as described herein. It is possible to provide WLP performance on glass at a much lower cost. The conductor features on glass are fine enough for the most demanding packaging and assembly techniques. The lowered cost of glass applies to the interconnection circuit plus assembly, test and rework. A test method called Tester-On-Board (TOB) is proposed, employing special-purpose test chips that are directly mounted in the system and mimic the capabilities of external testers. Methods for hermetic sealing, electromagnetic screening, and high-density off-board connections are also proposed.

Keywords: WLP, stud bump, hermetic module, shielded module, glass panel manufacturing, release layer, compliant packaging, thermal package, high-density interconnect (HDI), Tester-On-Board (TOB).

1. INTRODUCTION

The author was researching new structures for non-impact printers at a previous company[1]. The desired resolution was 1240 dots per inch which corresponds to a pitch of 20 microns per pixel. A 12-inch wide print head was also desired, so fine features were required on large substrates. The company turned to LCD panel manufacturers to fabricate the circuits on glass panels measuring approximately 16 x 22 inches. It was not difficult to produce sub 5-micron features on the glass panels. Later, printing through membrane apertures was also explored, using polyimide on glass as the membrane. It was observed that fine conductor features on the polyimide were still achievable. It is postulated that the glass carrier provides the mechanical support and dimensional stability required to produce fine features on a flexible coating, providing it is not too thick. The proposed total thickness for SysFlex circuits is around 50 microns.

Today, most glass panels are manufactured in the Western Pacific Rim. Seventh generation LCD fabs have been announced for producing panels that are 1800 x 1500 mm in area. This is 38 times larger than a 300 mm wafer. It enables large circuit boards as well as low cost per unit area. Industry sources have provided cost data for rough estimates. The estimated cost for 7-mask glass processing is $0.25 per square inch for a fully loaded fab. If a 12-inch wafer costs $300 for 2-mask WLP, the ratio of silicon cost to glass cost is 10, compared using dollars per square inch of processing. With WLP, the only thing provided for this price is a small package; the system producer still needs a motherboard for integrating his WLP components. This is included however, in the cost quoted for glass, because the glass-based circuits include both the circuit board and the "package". Also, the glass-based product can be denser and more highly integrated, particularly through the use of thin film transistor (TFT) arrays, as will be further described in this paper. These observations were the starting point for SysFlex. The author's background includes system engineering as well as semiconductors and printers, and he is motivated to look for ways to integrate or unify the steps of fabrication, assembly, test and rework. So, starting with the fine-featured capability of polyimide circuits on glass, he has researched potential approaches for building electronic modules at low cost, including attention to hermeticity, electrical noise, and thermal design issues.

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2. GLASS PROCESSING

The first liquid crystal displays (LCDs) were introduced for electronic calculators in the early 1970s. Since then, spanning 7 generations of development, the edge dimension of glass substrates has increased from 150 mm to 1800 mm and glass processing has become a mature manufacturing business. Today, a 7-mask process is employed to build the active matrix substrate of an active matrix liquid crystal display (AMLCD). "Active matrix" refers to the thin film transistors (TFTs) that control the pixel-based display elements.

If the required functionality of a component is driven by logic or memory capabilities, then the cost and performance of silicon-based transistors cannot be improved on. However, electronic systems generally require human interfaces like displays and keyboards, and for these, size is important. Also, transducer arrays may require a large size for collecting or generating the signal. In these applications, glass processing can be an attractive option, with the cost per unit area only a few percent of the cost of silicon. In addition, circuit boards are required for integrating IC chips into systems, and glass processing may offer the best manufacturing approach for making those boards.

Glass substrates have several inherent advantages. They start out as a molten liquid, and the effect of gravity on the melt is to form a very flat surface. Forming processes have been developed to create large substrates with good dimensional stability. Some substrates are manufactured to meet the stringent surface requirements of AMLCD manufacture without any grinding or polishing. There is also potential for re-using the glass carriers, together with their release layers.

2.1 Glass Panel Layout

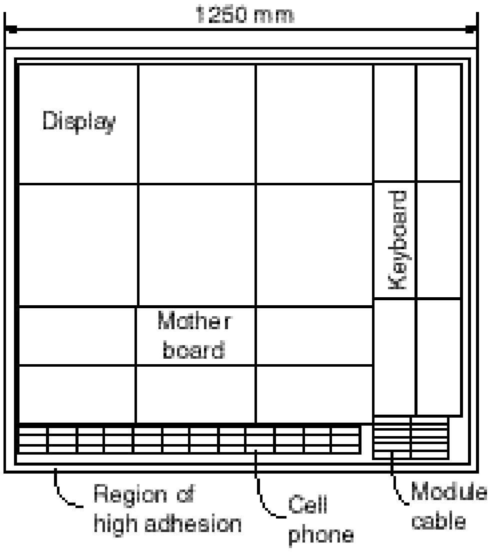

Figure 1: Glass panel layout for mobile computer

This panel layout represents 5th generation processing with a panel size of 1250 x 1100 mm. The primary target application is a mobile computer. The display and keyboard areas will become "roll up devices", as further described in the author's patent application[2]. After applying a release layer and a polymer base layer on the glass, conductive and dielectric layers are applied and patterned to create multi-layer interconnection circuits. Also, bonding sites are created for attaching IC chips by the flip chip method. After dicing with a diamond saw to separate the designated areas, IC chips are attached as required. The methods relating to the interconnection circuits, bonding sites, and IC chip assembly will be further developed in this paper. The display area will typically be further processed by applying organic electro-luminescent materials to form an organic light emitting diode (OLED) display. Ink-jet printers may be employed to apply a small spot of material for each color at each pixel location. The module cable is included because it requires fine features to support a pad pitch of 100 microns or less for the module access port. It seems attractive to manufacture all of the necessary components with the same base process. The presence of the cell phone circuit suggests potential flexibility in the business model. A manufacturer can mix and match circuits for multiple products and multiple customers on the large glass panels.

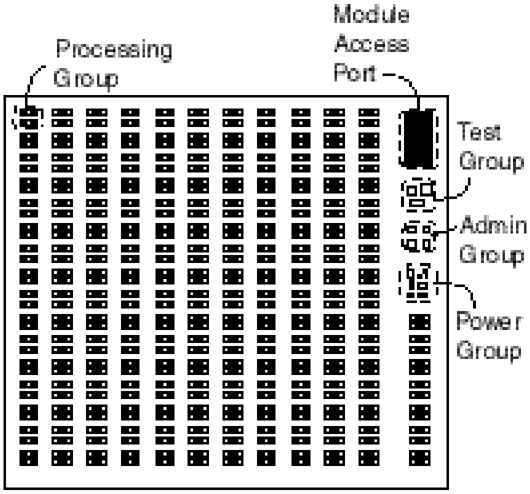

Figure 2: Glass panel layout for a blade server

Figure 2 shows an alternative layout for the glass panel. In this case, the entire panel is allocated to a single complex assembly comprising over a hundred processing groups configured as a blade server. Each processing group may include computational, memory, and communication chips. A module access port is provided for testing the interconnection circuits prior to assembly, as well as the chips of the test group, as further described in a second patent application[3]. The test group includes special-purpose programmable test chips. These chips are used to test the total function of the board at full speed, and with improved noise margins compared with using an external tester. The administration group employs background processes to oversee and manage the overall health of the blade server. The power group includes power-conditioning circuits, and the three support groups make the blade server a stand-alone unit that can be conveniently maintained or replaced. The compact form factor and the liquid-cooled configuration described in section 7 provide dense system capability.

2.2 Release Layer

A release layer is provided between the glass carrier and the interconnection circuit so that the carrier can be removed when most of the processing is done. The carrier adds bulk, weight, and rigidity that are usually detrimental in the final product. Also the presence of the glass may obstruct heat dissipation paths. Its purpose is to provide mechanical support and dimensional stability through fabrication of the interconnection circuits, preparation of bonding sites for IC chips, IC chip assembly, test, rework, and attachment of module access cables. After these steps are completed, the flexible substrate is peeled away from the glass carrier, and the carrier is discarded or set aside for re-use.

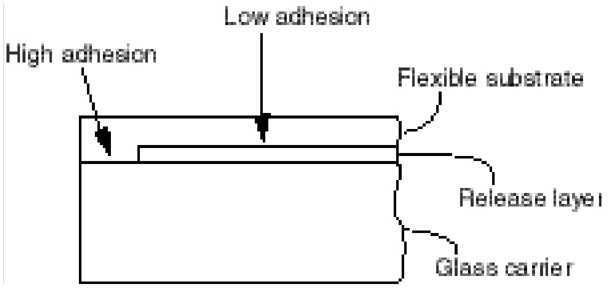

Figure 3: Release layer in relation to glass carrier and flexible substrate

Several choices exist for the flexible substrate material. Most polyimides such as Kapton can be processed at temperatures up to around 400ºC. Clear flexible substrates may be advantageous, especially for bottom-emitting OLED displays. Polyethylene terepthalate (PET) and polyether sulfone (PES) are clear and flexible, and can tolerate 200ºC. Accordingly, the industry is developing TFT processes that can be used with these materials, staying under the temperature limit, to provide active matrix display capability for movies and other dynamic display applications.

Work has begun for characterizing release properties of suitable materials. One promising construction is to use a fluorosilicone gel that behaves like a fluid as the parts are separated. Typically, the release layer contains a silane component that bonds well to the glass carrier but does not provide any organic bonds to the flexible substrate material, which is generally an organic polymer. This means that the carrier retains the release layer after separation, leading to the potential for re-use of the carrier plus release layer. An optional technique is to provide streets on the glass carrier where the release layer is absent. The streets provide regions of high adhesion to anchor the flexible substrate during processing. They can be trimmed just prior to separation, whether from the periphery of the full-size glass carrier, or from individual glass carriers corresponding to designated circuits.

3. INTERCONNECTION CIRCUIT TECHNOLOGY

At aggressive pad pitches, none of the printed circuit board technologies available today can provide direct bonding of IC chips to the interconnection circuit without a redistribution layer. Also, few if any of the available flip chip assembly methods can achieve reliable and low-cost rework of defective ICs. It is projected that glass-based circuits can overcome both of these problems. Firstly, because of their inherent fine-line capabilities, they can accept IC chips with pad pitches of 100 microns or less, with no redistribution circuits or intervening packages. Secondly, because the glass layer provides mechanical support and dimensional stability throughout the rework phase, the rework of defective ICs can be reliable and robust, despite the closely spaced bonding sites. This is further discussed in the next section.

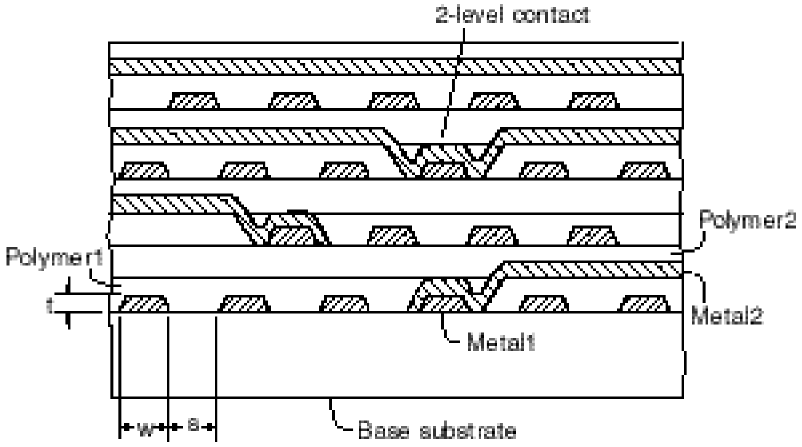

Figure 4: 8-layer flexible interconnection circuit

In Figure 4, aluminum traces have width, w, and space, s, both equal to 5 microns. Trace thickness, t, is 1 micron. Photo-imageable Cyclotene[4] is used for the polymer layers. Cyclotene is also known as benzocyclobutene (BCB). When exposed with light through a mask and subsequently developed, contact holes having sloping walls are formed in the Cyclotene. The sloping walls provide good step coverage of the subsequent metal layer. In principle, any number of layers can be provided; 8 layers are shown in the figure.

3.1 Stacked Contacts

Stacked contact structures are proposed, without requiring laser-drilled vias. Rather, the contact windows are etched with sloping walls using BCB, as described for 2-level contacts. Preferably, these contacts are provided only at bonding pad sites, where there is plenty of room for the larger contact structure. Stubs are provided at each metal layer, for subsequent routing as required. This strategy provides for minimum sized (2-level) contacts in routing areas away from the pads, leading to closely spaced parallel lines, yet with adequate routing capabilities.

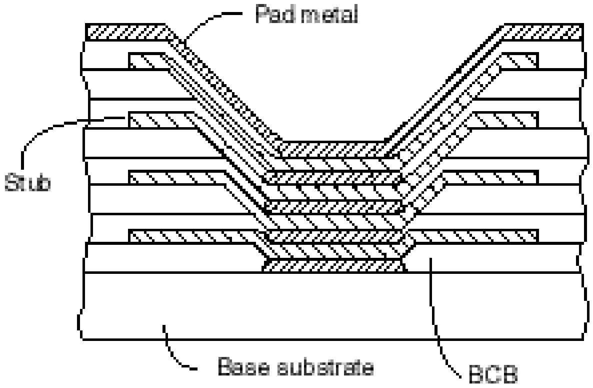

Figure 5: Stacked contact at a bonding pad

4. ASSEMBLY, TEST & REWORK

The overall objective is to achieve dense system packaging at low cost. The recent availability of gold stud bumping machines such as the 8098 bonder from Kulicke and Soffa has provided a great leap forward. Such machines are capable of forming stud bumps in large arrays, with bonding pitch less than 100 microns, and cost per stud bump of less than 0.03 cents. This is based on Kulicke and Soffa data for an 8-inch wafer with 200,000 bumps. The planarity of the gold tips is held to just a few microns across a 12-inch wafer, and the bonding rate is 12 stud bumps per second. Also, IC chips from multiple vendors can be prepared for assembly using a standard stud bumping process. This is preferably performed on wafers, but individual die can also be handled. Using 18-micron diameter gold wire, the stud bump can be configured to have a ball diameter of around 50 microns, and also a total height of around 50 microns. The beard is accurately sheared off to provide near-planarity of the tips.

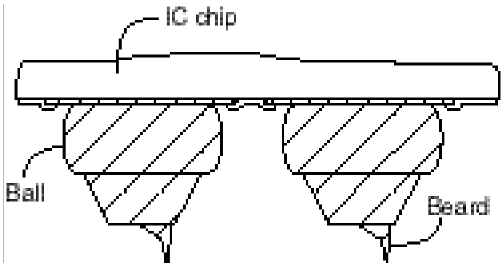

Figure 6: Gold stud bumps

A SysFlex motherboard is prepared for accepting the stud bumped devices by forming wells filled with solder, one well for each stud bump. A mask is formed using polyimide that is typically 15 microns thick, with openings above each input/output pad that are approximately 34 microns square. Solder paste is deposited in the wells using a squeegee. This is preferably accomplished using the full size glass panel, before it is diced into designated circuits, allowing several million wells to be filled using one pass of the squeegee. The cost per well is estimated at less than 0.02 cents, making the cost per flip chip bond less than 0.05 cents. Figure 7 shows the wells filled with solder paste.

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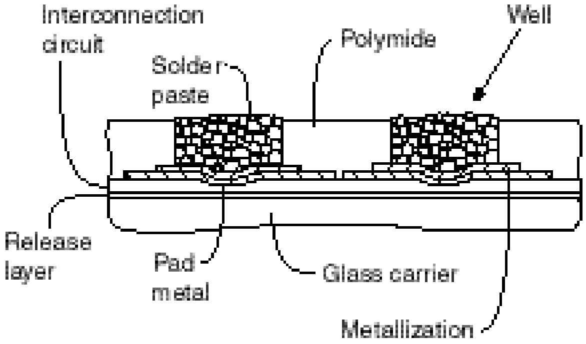

Figure 7: Wells filled with solder paste

The stud bumped device is aligned with the motherboard, and the stud bumps are inserted into the wells. The bonding pitch, P, can be 100 microns or less, as shown in Figure 8.

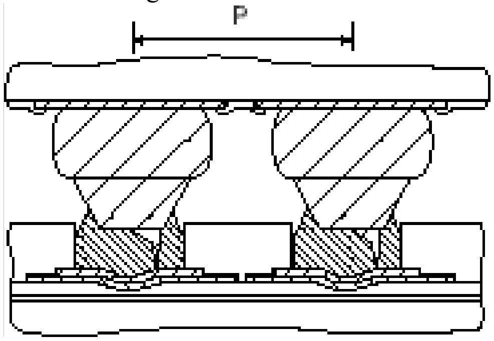

Figure 8: Completed flip chip connections

A slight modification of this structure can be applied to cables with stud bumps that are inserted into wells at module access ports. A module access port is included with each motherboard for testing purposes, as well as for connecting between the modules and other external systems. For example, at a bonding pitch of 100 microns, a 4,000-node connection can be provided using a bonding area of only 0.4 cm^2.

4.1 Test Fixture

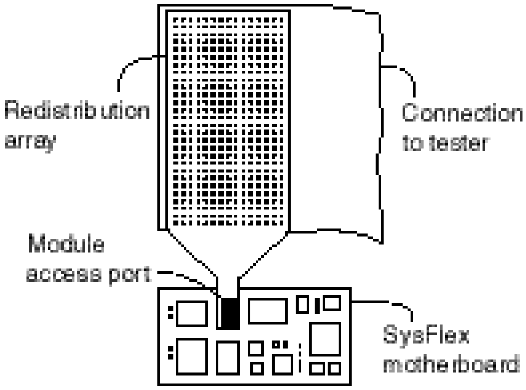

Figure 9: Test fixture for interfacing motherboard to tester

Figure 9 shows a test fixture connected to a module access port of a SysFlex motherboard. In this case, it may be convenient to retain the glass carrier with the test fixture. A flexible circuit connects to an external tester.

4.2 Assembly and test method

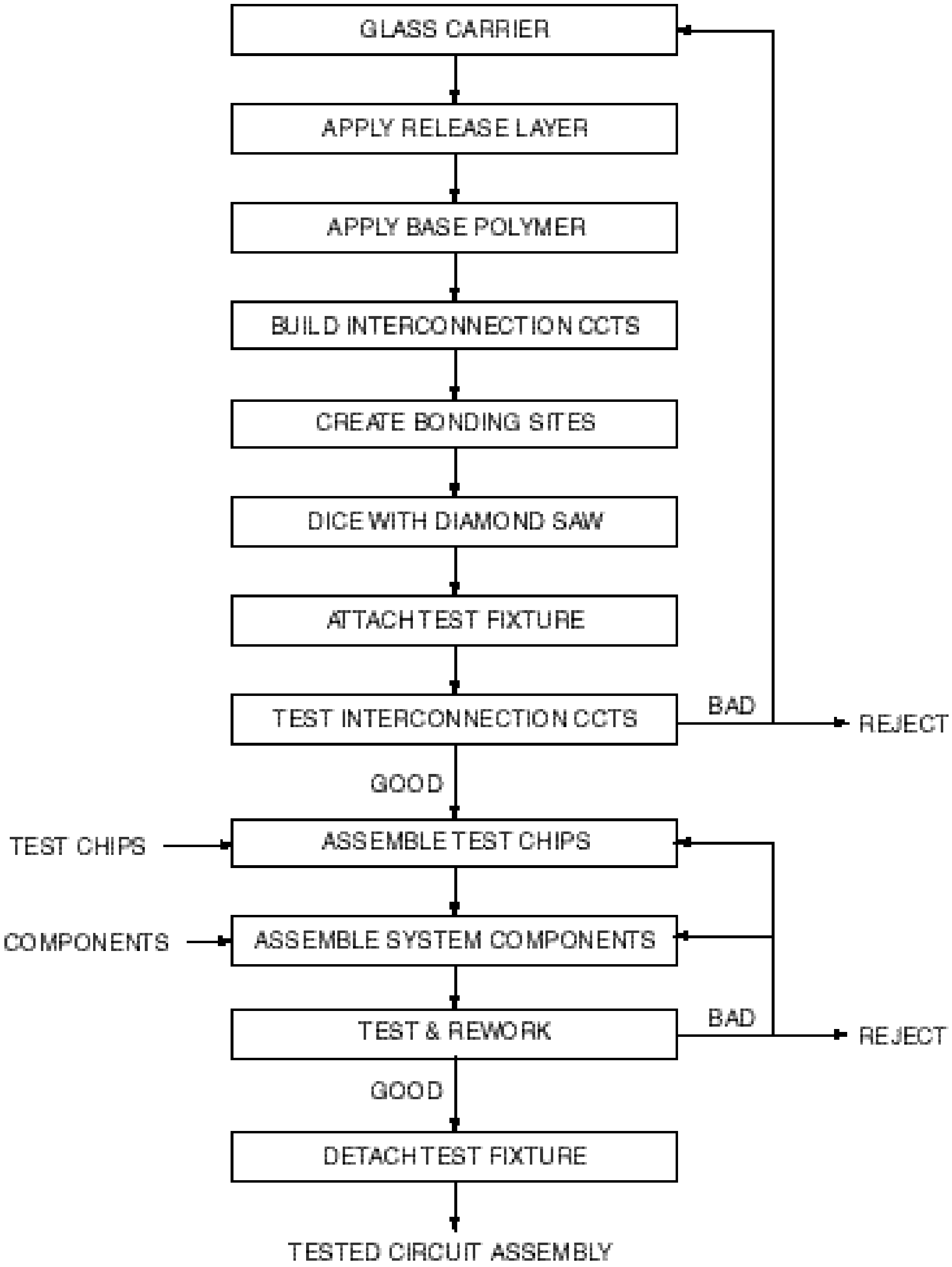

Figure 10: Flow chart of assembly and test method, including Tester-On-Board.

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The interconnection circuit is preferably tested with 100% fault coverage using the module access port. The test chips and the full complement of system components are attached. Where possible, discrete components like resistors, capacitors and inductors are created using thin film structures on glass or silicon substrates, and provided with stud bumps for connection to the motherboard. Recent fractal technology[5] may help to eliminate discrete components in RF circuits. Before assembly, each component is thoroughly tested to meet its own specification, usually without regard to the intended application. After assembly however, it is desirable to test only those requirements that pertain to the system level requirements of the current product, a tiny subset of all possible tests. This confines attention to failure modes that are relevant, and shortens test time.

More accurate and complete testing of components is provided when they are tested in their system environment rather than individually. The system environment is created with the actual system rather than a simulation created by test vectors programmed into a general-purpose tester. This can lead to lower test cost and faster test development, by using a high level language and eliminating the need to generate and debug detailed system response patterns.

The system can be verified at an elevated temperature by heating the glass carrier underneath the circuit assembly. This also provides a convenient method for performing accelerated life testing.

If convenient and reliable rework is achievable, then assembly and test operations can be co-located, and optimized as closely coupled processes. If a SysFlex part requires rework, it is heated by the application of hot inert gas and removed by lifting the stud bumps out of the wells. Touchup may require cleaning of the bonding surface between wells, and addition of solder paste. Then a new part can be selected and attached. Because the materials can easily tolerate the solder melting temperature, and because the glass carriers maintain good dimensional stability, this process can be repeated as often as necessary, even with a tight bonding pitch.

The concept of Tester-On-Board (TOB) has only recently become feasible. It is enabled by the fact that modern test devices can be developed to mimic the capability of external testers, while placed directly in the system in the form of special-purpose test chips. Most of the complexity of current testers relates to pin electronics designed to overcome the problems of interfacing system nodes to tester nodes through cables, relays and connectors. This problem gets worse as speeds increase and operating voltages diminish. It is preferable to exercise the system using high-level system code, using the environment of the actual system, while capturing and validating the behavior with local sensors (test chips) mounted directly alongside the system components. The test program becomes a version of the user program, taking care to exercise all of the system capabilities. If digital, analog, and RF functions are required, then multiple test chips will be necessary. However, adding these test chips to the system using the SysFlex approach is not as expensive as in the past because the production volume of these chips will be high, leading to low unit costs, and the cost of packaging and assembly will be minimal. A tester is included with every module produced, but its cost may be redeemed by more efficient production, shorter time to market, and improved usability of fielded products. Imagine a laptop that can warn you just before it gets too hot, or a cell phone that can detect a dropout before you hear it and adapt by temporarily boosting power to critical circuits. Currently, the cost of testing is typically around 4% of manufacturing cost. If 1 out of 25 system chips are test chips, representing less than 4% of total manufacturing cost, it is possible that finished system costs will be lower than those achieved with conventional testing methods.

5. ACTIVE MATRIX ARRAYS USING TFTS

The AMLCD process that represents the bulk of glass processing today includes the capability to manufacture arrays of TFTs. SysFlex processes can include TFTs for those applications that require it. The combination of high-performance silicon chips in a compact form factor with lower performance TFTs in a distributed form factor is a powerful combination that can be applied to displays, keyboards, sensors, and transducers of many kinds.

An example 7-mask TFT process is shown in Figure 11, as documented by AKT, Inc. If combined with SysFlex technology, the masking steps would be modified to optimize the total process.

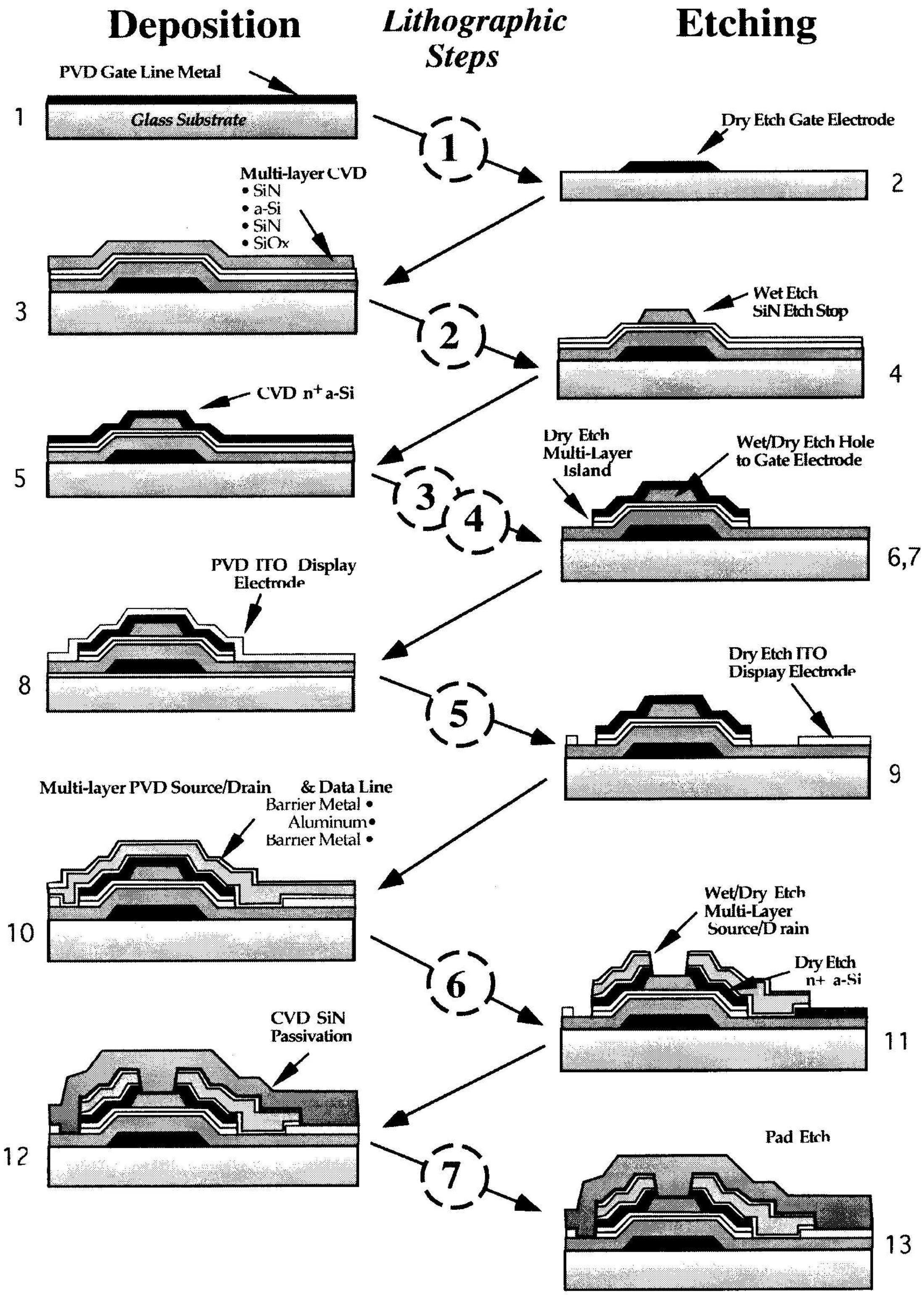

Figure 11: An example TFT process, following AKT, Inc.

5.1 Pixel display circuits employing TFTs

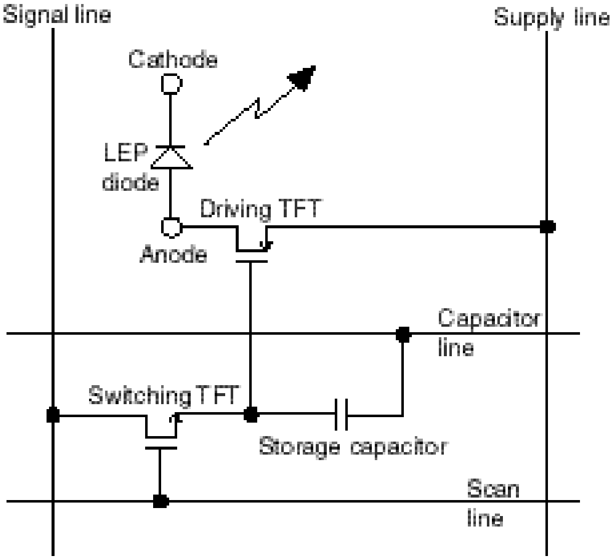

Figure 12: An example pixel display circuit, following Cambridge Display Technology

Figure 12 shows an example pixel circuit developed by Cambridge Display Technology[6] of Cambridge, UK. This type of display is capable of high resolution, large size, and fast refresh rate, although the OLED processing is not yet mature. The light emitting material is referred to here as a light-emitting polymer (LEP). An array of pixel circuits such as shown in Figure 12 is referred to as the display back plane. It can be implemented using a combination of SysFlex technology and TFT technology.

5.2 Touch sensing circuits employing TFTs

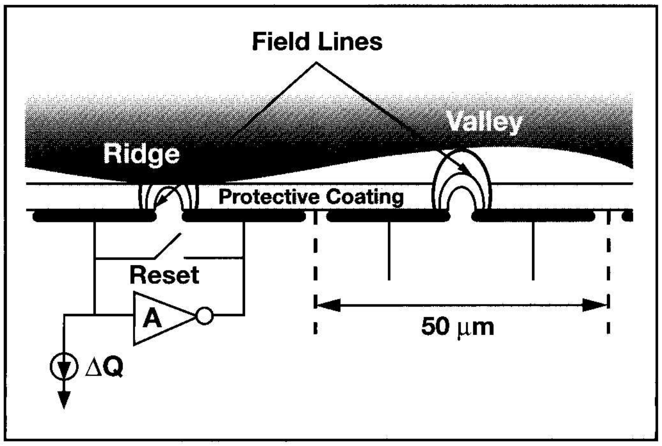

Figure 13: Touch sensing circuit developed by STMicroelectronics.

Figure 13 shows the repeating circuit for a fingerprint sensor developed by STMicroelectronics[7]. Similar technology can be adapted for multiple touch sensing applications, including keyboards, touch pads, and fingerprint sensors. A charge integrator is implemented wherein the sensed capacitance, differing between a ridge and a valley of the user's fingerprint, is converted to an output voltage. The fine features of SysFlex may be employed to create higher resolution sensors than shown in Figure 13. The inverter and reset switch can be implemented with TFTs, as wells as row and column addressing switches. Multiple capacitance sensing devices can also be arrayed with multiple display devices, each incorporating a matrix of TFT devices, for advanced human interface applications.

6. MODULE LEVEL PACKAGING

It is customary to worry about electrical noise problems and the effects of humidity after the system is built. If hermetic systems are required, then bulky and expensive packages are normally provided for each component. If low electromagnetic radiation (EMR) is required, then metal boxes are often provided to enclose critical components. Unfortunately these strategies may not be effective, because some problem devices may not be identified until the last minute, when system qualification tests are performed. There may however be an opportunity to address these issues at the module level rather than at the component level, wherein every component is protected, as part of a standard manufacturing process. In particular, a continuous coating of metal around the substrate and the attached parts may be an effective water barrier and an effective electrical screen. The proposed coating is aluminum, with a thickness of at least one micron. The module cannot be totally enclosed with metal because of the necessity to provide a means for communicating with the module. A semi-hermetic module access port is proposed for this purpose.

R. K. Traeger[8] has documented the water permeabilities of silicones, epoxies, fluorocarbons, glasses, and metals. His data shows that, in terms of providing a barrier to water, a layer of metal that is 1 micron thick is approximately equivalent to a layer of glass that is 1 mm thick, and also equivalent to a layer of epoxy that is 100 cm thick. Methods are available for coating around all sides of a circuit assembly, using either sputtering or evaporative techniques. A typical result is shown in Figure 14.

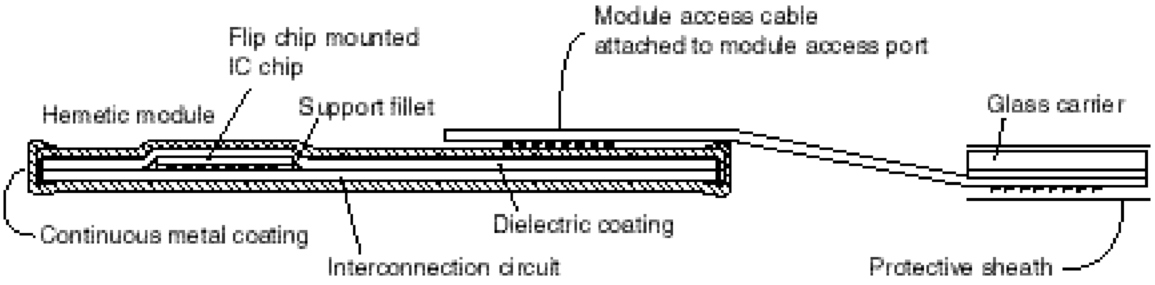

Figure 14: SysFlex module with attached module access cable.

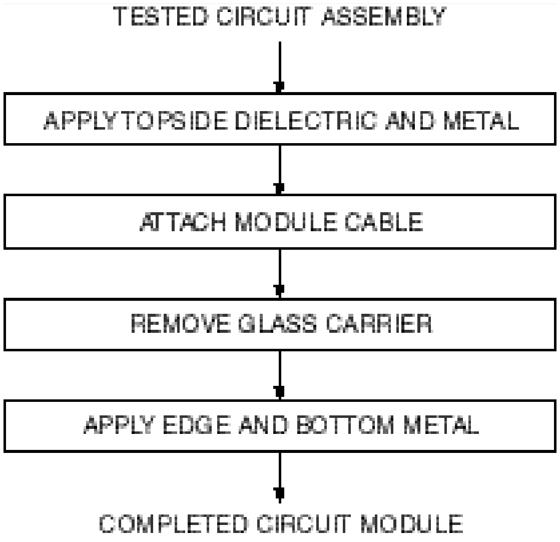

Figure 15: Flow chart for module packaging layers.

7. ADVANCED THERMAL CONFIGURATION

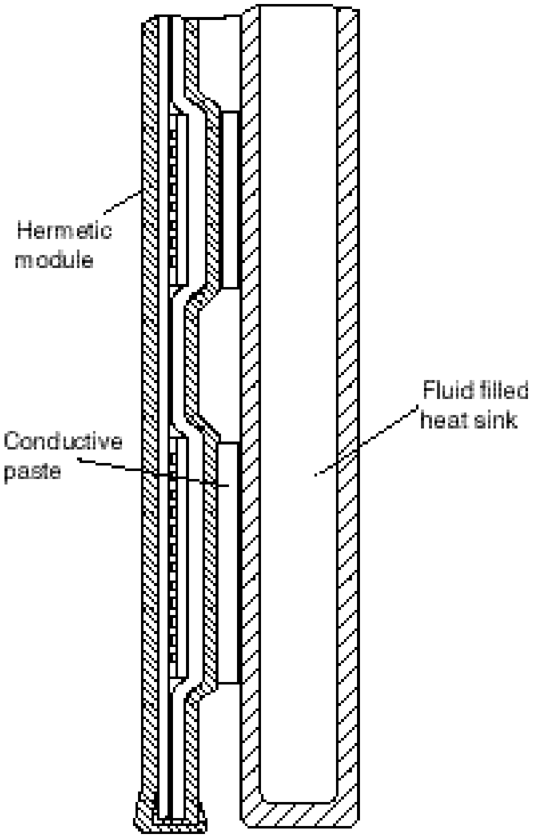

Figure 16: Water-cooled blade server configuration

Figure 16 shows a thermal design for cooling a blade server. The thermal path from the active junctions of the IC chips to the cooling fluid has low impedance. It may be possible to modularize the plumbing and electrical connections, to make a high performance replaceable unit.

ACKNOWLEDGMENTS

Prior work on non-impact printing structures provided the basis and illuminated the possibilities for fine-featured flexible circuits. This work was performed at The Salmon Group, LLC, Los Altos California, and was funded primarily by David M. Salmon. I'd also like to thank Dann Gustavson for his review and insightful comments on testing.

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