



# Advanced System Packaging

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- Glass processing
- Interconnection circuits
- Assembly methods
- Testing
- Module integration
- Summary

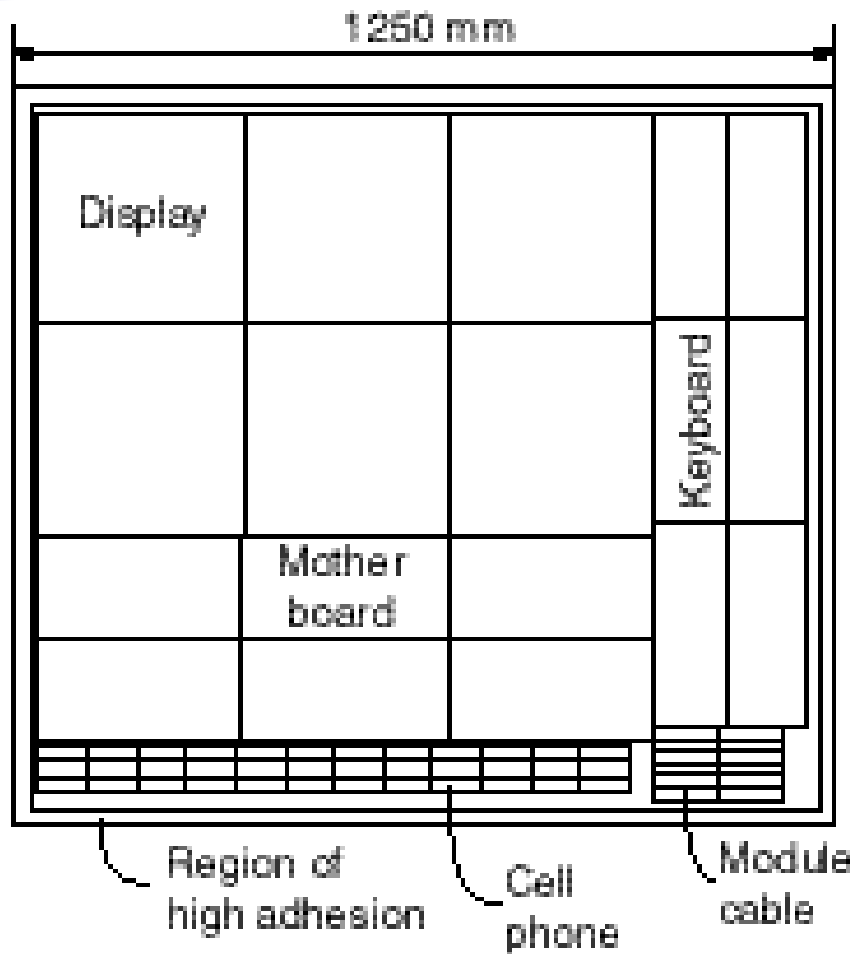


# Glass Processing (1)

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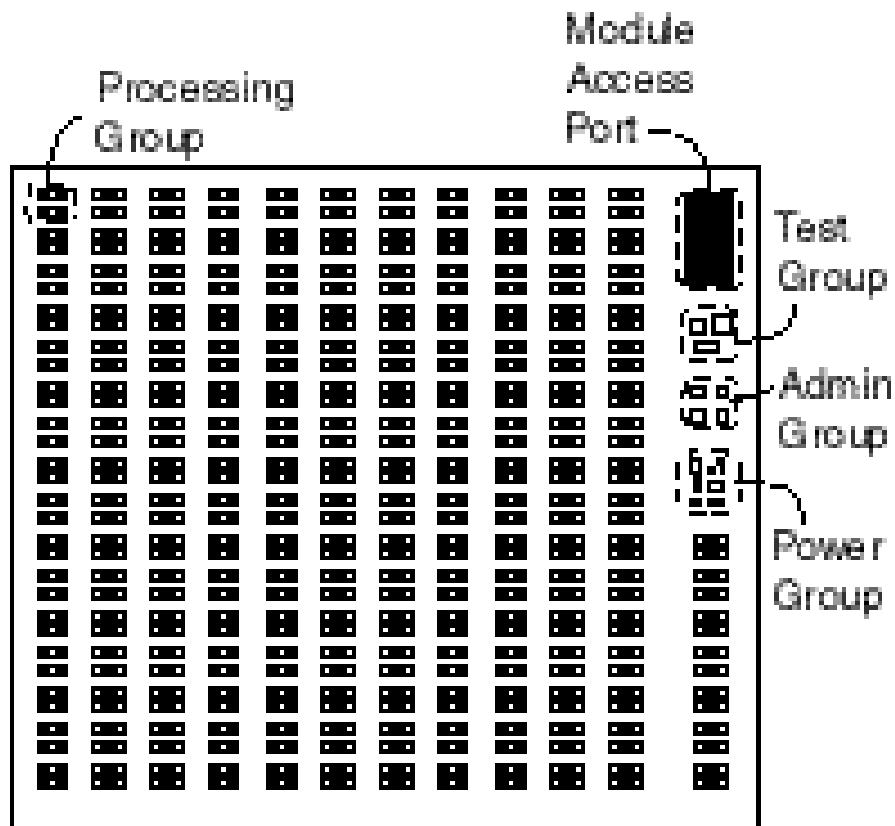
- LCD manufacturing is mature:
  - Currently at 7<sup>th</sup> generation
  - Panel size up to 1800 x 1500 mm
  - Integrated thin film transistors (TFTs)
  - SysFlex adds new capabilities:
    - Integration of IC chips and TFT circuits
    - Improved testing of high speed systems
    - Moisture protection & low EMR

# Glass Processing (2)



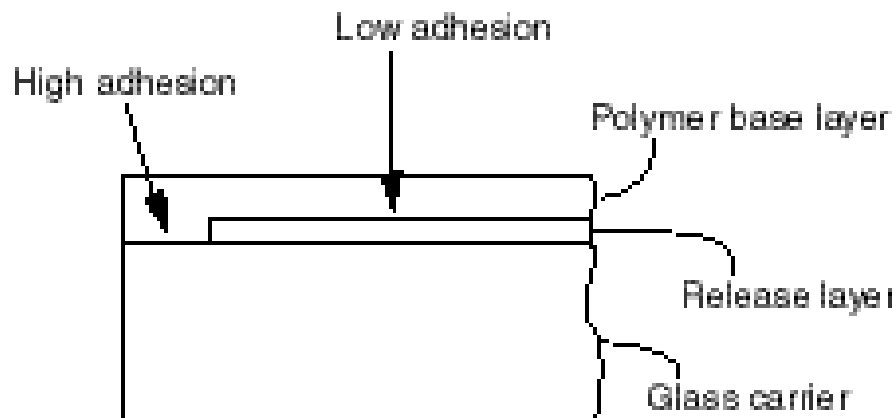
- 5<sup>th</sup> generation panel
- Mix and match
  - Circuits
  - Customers

# Glass Processing (3)



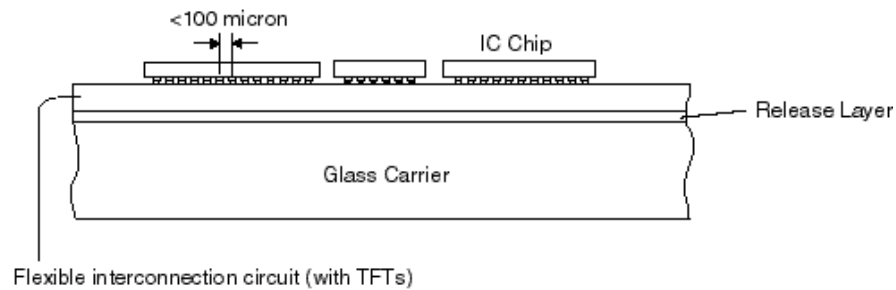
- Blade server
- Supercomputer
  - Rework enables several hundred processors/panel
  - Advanced cooling option available

# Glass Processing (4)



- Anchor at edges
- Peel center portion
- Separate designated circuits with diamond saw

# Glass Processing (5)



- Assemble, test, rework and attach cables
- Then separate carrier

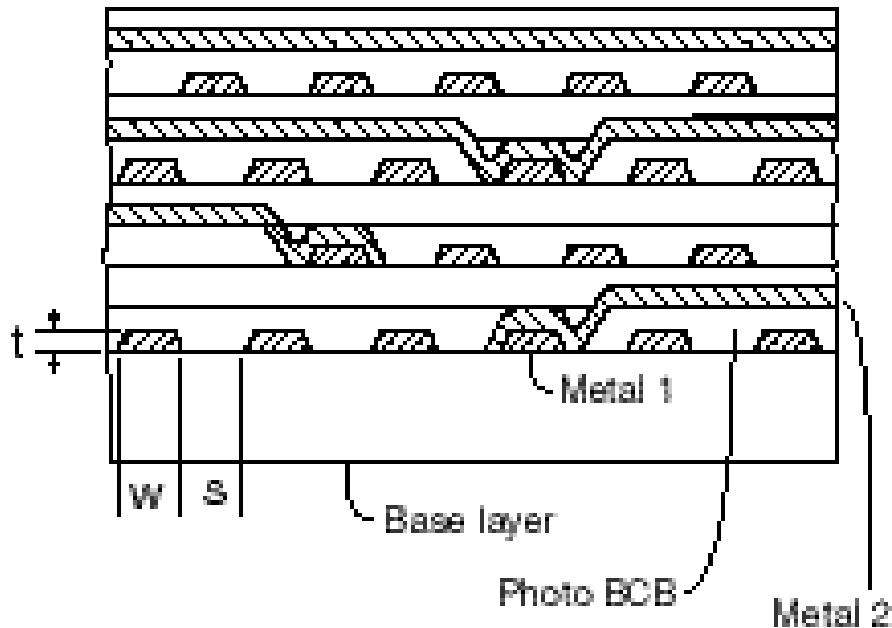


# Glass Processing (6)

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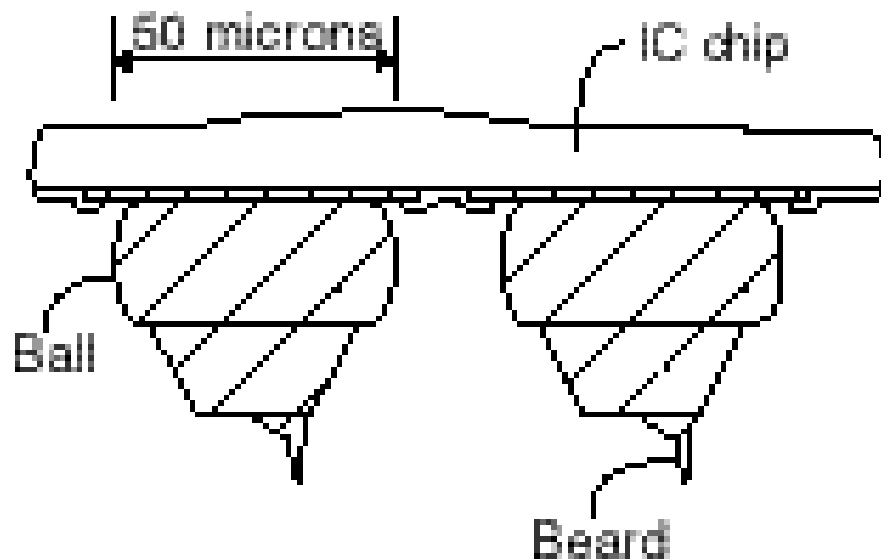
- Cost data from Samsung Electronics
  - \$1.39/in<sup>2</sup> in 2002 (15" display panel)
  - \$1.10/in<sup>2</sup> in 2005 (19" display panel)
- SysFlex 10-layer -> \$0.40/ in<sup>2</sup> in 2005
- Compare, \$0.43/ in<sup>2</sup> for 8-layer Cu PCB
  - Cannot directly attach IC chips
  - No TFT capability

# Interconnection Circuits



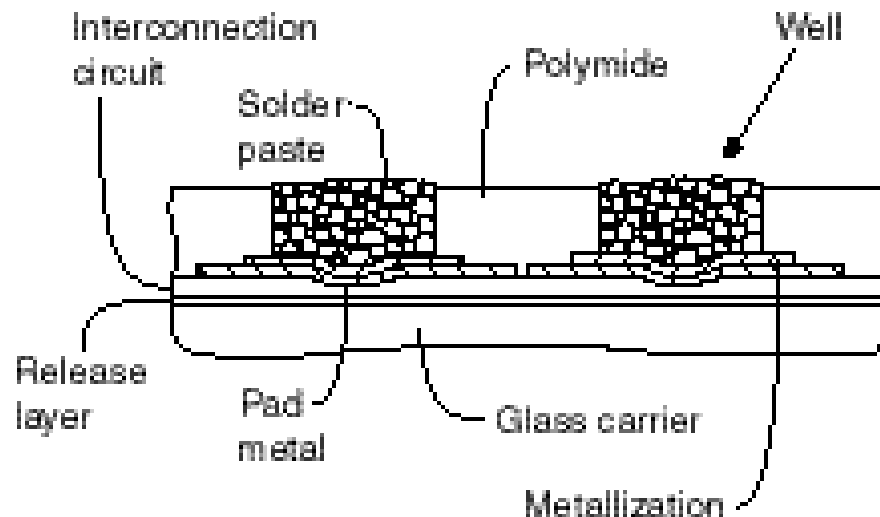
- $W=S=5\mu$
- 8 or more layers
- Stacked contacts
  - No drilled vias

# Assembly Method (1)



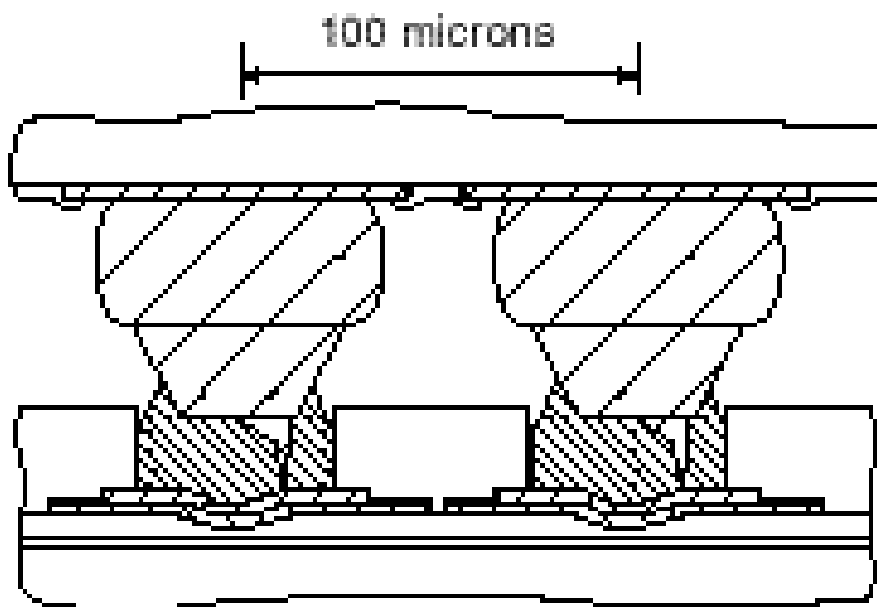
- Gold stud bumps
- K&S 8098 bonder
- Wafers or chips
- Excellent planarity
- 0.03 cents each
- 12 stud bumps/sec

# Assembly Method (2)



- Tens of millions of wells/panel
- One pass of squeegee
- 0.02 cents/well

# Assembly Method (3)



- Pitch =  $100\mu$  or less
- Re-workable using non-heroic methods
- Cost/bond =  $0.05\text{¢}$ 
  - $\ll 1.0\text{¢}$  benchmark
- No under-fill required
  - Compliant package

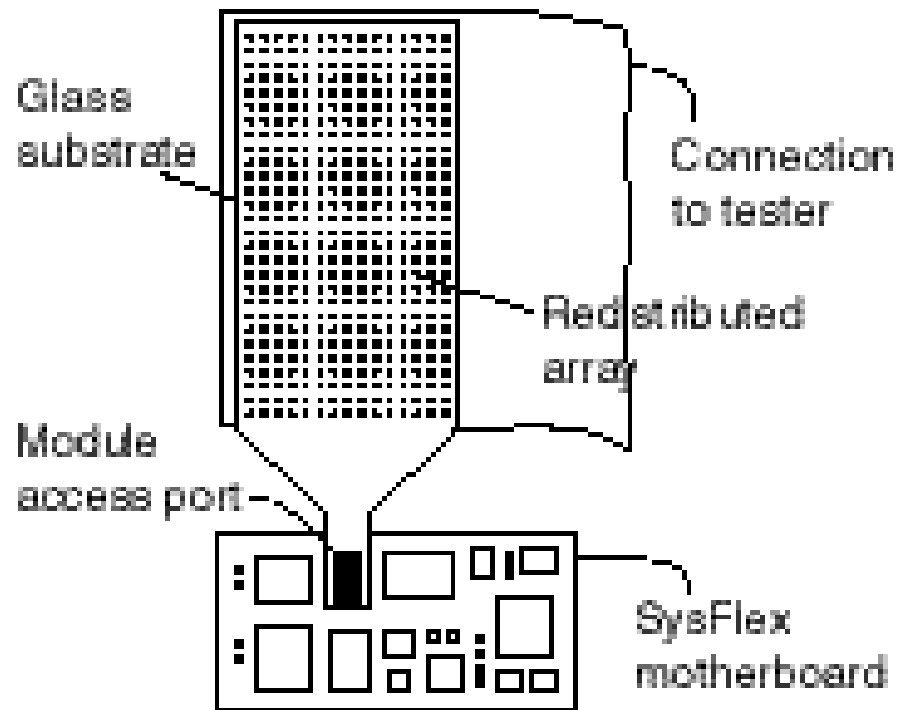


# Tester-On-Board (TOB)

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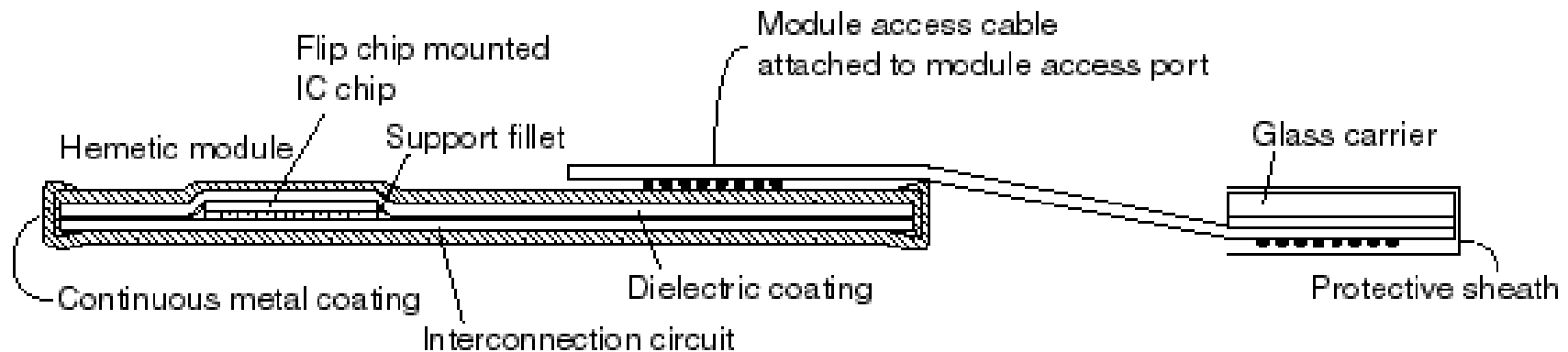
- Test chip or chips on system board mimic capabilities of external testers
- Eliminate difficult pin electronics
- Improve test speed and noise margin
- Low cost to implement
  - Chip cost is lower in high volume
  - Assembly cost is minimal
- Improved usability of system

# Test Fixture - I/O connections



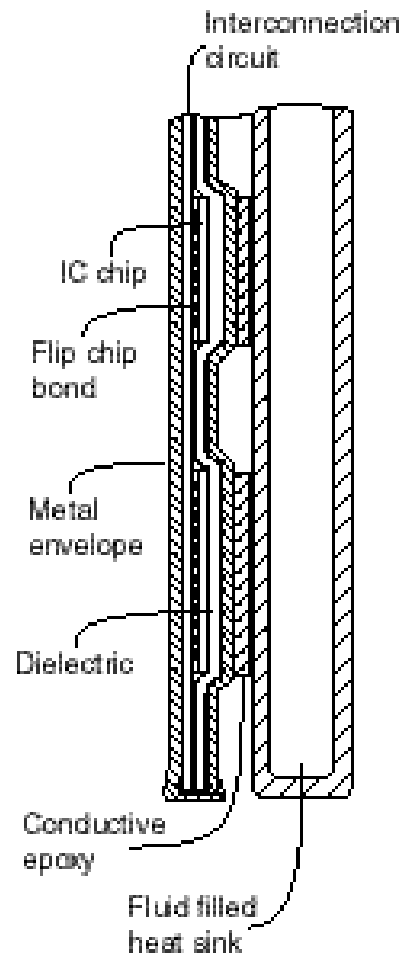
- Apply 100 $\mu$  pitch to off-board connections
- 10,000 I/O per sq.cm.

# Module Integration (1)



- Metal coating envelopes module
  - Excellent water barrier + Low noise
  - Protection is built in *by design*

# Module Integration (2)



- Very low  $\theta_{JC}$
- Modularize plumbing
- Module < 1cm thick



# Summary

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- Higher system integration requires
  - More complex SOC, or
  - Better integration fabric
- More complex SOC has severe problems
  - Digital + Analog + HF
    - Additional masks are expensive
    - Design time can increase exponentially
- SysFlex is a potent solution
  - Density    Testability    Assembly    Cooling    Noise  
Hermeticity    Design Time    System Cost