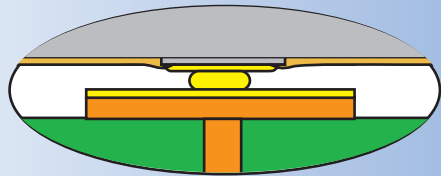
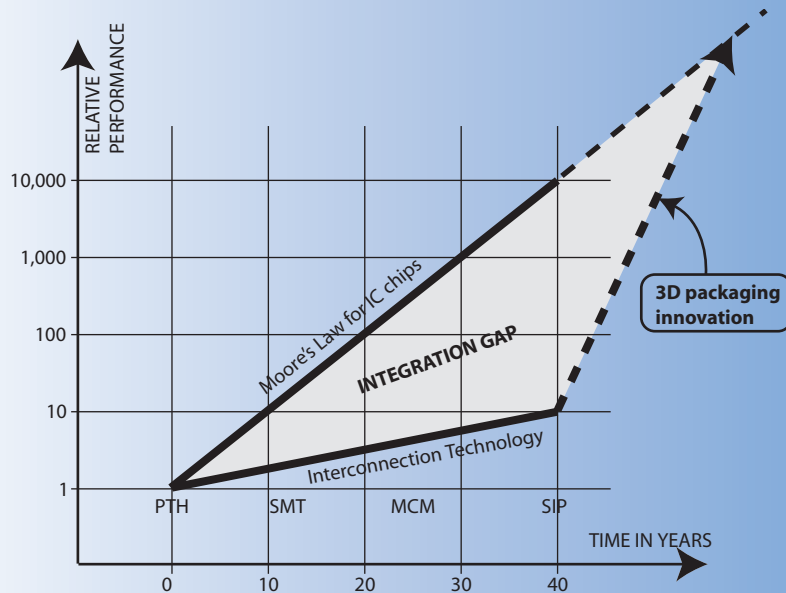


3D Packaging Technology



Gold stud bump innovation



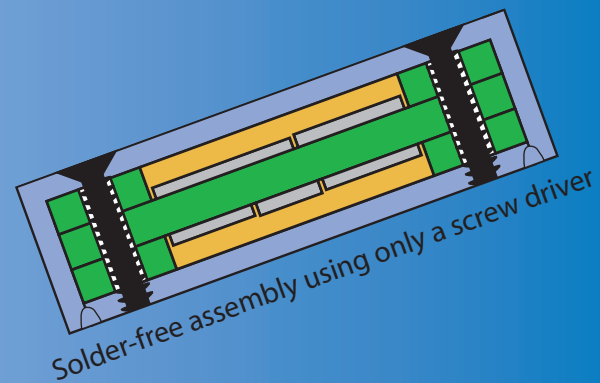
Freedom to operate

Short time-to-market

Lowest cost solution

Use existing die

Works for all electronic systems



Mar 2009, US Pat No 7,505,862, Apparatus and Method for Testing Electronic Systems
Sep 2009, US Pat No 7,586,747, Scalable Subsystem Architecture ... Cooling Channels
Sep 2008, US Pat No 7,427,809, Repairable 3D Semiconductor Subsystem
Aug 2007, US Pat No 7,254,024, Cooling Apparatus and Method
Additional patents issued and pending