



PETER SALMON

Peter C. Salmon, LLC

1885 S. Springer Rd. #B

Mountain View, CA 94040-4052

(650) 814-1076 (cell)

<http://petersalmon.com> (website)

peter@petersalmon.com (email)

www.californiaconsultants.org (IEEECNSV)

<http://www.linkedin.com/in/petersalmon2008>

Engineering Consulting Systems Design & Product Development Semiconductor Packaging

CAREER PROFILE

Broad operating experience in senior technical roles at Fairchild, Intel, ESL/TRW, GTE, and three startup companies spanning the semiconductor, printing, and defense industries. Author and owner of over 20 patents. Board member of Silicon Valley Consultant's Network, CNSV, a special interest group of IEEE.

EXPERIENCE

- **Semiconductors:** Designed multiple custom integrated circuits, hybrid assemblies, and manufacturing processes. Developed advanced technology for integrating semiconductors into systems, including a new flip chip connector, a novel cooling method, a new test methodology, and a solder-free assembly method. Developing new technology for HDI interconnection substrates supporting a pad pitch as small as 40 μ m. Have emphasized the fundamental importance of effective rework strategies for locating and replacing defective components in systems. Wafer and panel level processing, including automation for low cost production.
- **Expert Witness:** Founder and Co-chair of the Intellectual Property group at Consultants' Network of Silicon Valley. Member of Silicon Valley Expert Witness Group, Round Table Group, and National Expert Witness Network. Litigation support, patent evaluation, and product tear-down experience.
- **Patent Author:** Learned the art of patent writing from the late Aldo J. Test. Experience relates to technology, prosecution, and associated business development. Author of over 20 patents. In 2007 sold a group of patents to an Asian manufacturer.

WORK HISTORY

10/2010 – Present

Sagalio, Inc.

Founder and CTO

- Developed a new approach to roll-up devices in the mobile space
- 7 patents pending

7/2001 – Present

Peter C. Salmon, LLC

Engineering Consultant

- Systems Engineer
- Product Developer
- Litigation support expert
- Created a broad portfolio of patents relating to integrating semiconductors into electronic systems. Systems may consist almost entirely of bare die. System solutions span structure, cooling, and testing, and also include solder-free assemblies.

11/1997 – 6/2001

The Salmon Group, LLC

Founder and CTO

- Invented and partially developed Solid State Printing, SSP, a new method for high performance digital printing that eliminates the optical subsystems of existing laser printers
- Leader of the development group comprising a core team of system engineers plus multiple consultants and suppliers
- Developed a novel semiconductor process for the print heads

6/1991 - 11/1997

TRW

Senior Staff Engineer - Systems

- Led the Engineering Automation Group
- Developed processes for requirements management and thread modeling
- Co-founded and chaired a working group called Model Driven System Design under INCOSE, the International Council of System Engineers
- Systems engineer on several Reconnaissance Systems
- Generated multiple proposals and system specifications

7/1989 - 6/1991

GTE Government Systems

Section Head

- Managed Reconnaissance Systems Group of 13 engineers
- Co-developed a behavioral model for a \$100M reconnaissance system and used it to drive the system software architecture
- Active in risk management training, OOD, CORBA

6/1986 - 7/1989

ESL, a subsidiary of TRW

Senior Member of the Technical Staff

- Performed in various technical roles such as Systems Engineer and Technical Director on programs from \$12M to \$23M
- Wrote highly regarded white paper on Search System Performance

4/1984 - 5/1986

Source III

VP Business Development

- Developed library of standard cells for ASIC development
- Negotiated foundry agreements with 7 wafer manufacturers
- Wrote manual for first-time users of cell-based ASIC tools

9/1979 - 2/1984

Santek

Co-founder & VP Engineering

- Developed and patented new thermal printer with integrated dot-driver ICs
- Designed and developed several full-custom ICs
- Negotiated license agreement with Kyocera

4/1974 - 8/1979

Intel

Staff Engineer

- Developed support chips for the 8080 microprocessor family
- Group leader for engine control circuits
- Developed and patented novel concept for video games
- Taught graduate electronics course at Santa Clara university

6/1971 - 4/1974

Fairchild Semiconductor

Chip Design Engineer

- Logic and circuit designer for several calculator chips

EDUCATION

1972 Northeastern University, Boston

Electrical Engineer, a professional degree

Major: Device Physics; Minor: Materials Science

1969 Northeastern University, Boston

Master of Science in Electrical Engineering

1967 Auckland University, New Zealand

Bachelor of Electrical Engineering

AFFILIATIONS

- Institute of Electrical and Electronic Engineers (IEEE), CPMT & CNSV chapters
- IEEE CNSV, Consultant's Network of Silicon Valley, Board Member
- SVEWG, Silicon Valley Expert Witness Group
- RTG, Round Table Group
- NEWN, National Expert Witness Network
- TAEUS, Expert Witness Group
- MEPTEC, Micro-Electronic Packaging and Test Engineering Council
- Inventor's Alliance, Bay Area Chapter

RECENT PRESENTATIONS & PUBLICATIONS

- *PATENT AND INVENTION STRATEGIES - GOOD WAYS TO SPEND YOUR TIME AND MONEY*, a half-day webinar presented by IEEE- CNSV, September 17, 2010.
- *FUZE ELECTRONICS MINIATURIZATION*, white paper, March, 2010.
- *MAGNAVOX AND INTEL: AN ODYSSEY*, co-authored with Stan Mazor, IEEE Annals of the History of Computing, September, 2009.
- *PATENT LANDSCAPE ANALYSIS, SERVERS AND DATA CENTERS*, white paper, June, 2009, updated June 2010.
- *SOLDER-FREE CONNECTORS USING BUCKLED PILLARS*, feature print article, The MEPTEC Report, December, 2008.
- *SOLDER-FREE CONNECTORS USING BUCKLED PILLARS*, web article, Advanced Packaging, September 23, 2008, http://ap.pennnet.com/articles/article_display.cfm?ARTICLE_ID=339446
- *HIGH PERFORMANCE MODULES ON COPPER SUBSTRATES: NEXT GENERATION PACKAGING FOR SERVERS AND SUPERCOMPUTERS*, IEEE CPMT Dinner Meeting, Sunnyvale, California, May 14, 2008.
- *HIGH PERFORMANCE MODULES ON COPPER SUBSTRATES: Meptec's 4th Annual conference: The Heat is On*, Sunnyvale, California, February 28, 2008.
- *COPPER PANEL FABRICATION AND STACKING CONCEPT FOR VLP FB DIMMS*, 3rd International Wafer Level Packaging Conference, San Jose California, Nov. 1-3, 2006.
- *COPPER PILLAR WELL METHODOLOGY AND IMPLEMENTATION IN A VLP FB DIMM*, 2006 KGD Packaging & Test Workshop, Napa California, Sept. 10-13, 2006
- *THE WORLD THROUGH THE EYES OF AN INVENTOR*, IEEE CNSV Dinner Meeting, Sunnyvale, California, April 18, 2006.

- *REPAIRABLE 3D SEMICONDUCTOR SUBSYSTEM**, 2nd International Wafer Level Packaging Conference, San Jose California, Nov. 3-4, 2005.
- *NOVEL SiP DESIGN CONCEPT: STACKED COPPER BGA*, 1st International Wafer Level Packaging Conference, San Jose California, Oct. 10-12, 2004.
- *FLIP CHIP CONNECTIONS USING BUMPS, WELLS, AND IMPRINTING*, IPC Printed Circuits Expo, Apex, and the Designer's Summit, Anaheim California, Feb. 24-26, 2004.
- *ADVANCED SYSTEM PACKAGING METHOD*, 4th International Symposium on Quality Electronic Design, IEEE, San Jose California, Mar. 24-27, 2003.
- *CHIP ON FLEX WITH 5-MICRON FEATURES*, Proceedings of SPIE, Micromachining and Microfabrication Process Technology VIII, San Jose California, Jan. 27-29, 2003.

* Best in Conference award.

ISSUED PATENTS

NO.	US Patent	
1	7,586,747	Scalable Subsystem having Integrated Cooling Channels
2	7,537,107	Tiled Construction of Layered Materials
3	7,505,862	Apparatus and Method for Testing Electronic Systems
4	7,427,809	Repairable three-dimensional semiconductor subsystem
5	7,415,289	Apparatus and method for deploying an information retrieval system
6	7,408,258	Interconnection circuit and electronic module using same
7	7,297,572	Fabrication method for electronic system modules
8	7,254,024	Cooling Apparatus and Method
9	7,163,830	Method for temporarily engaging electronic component for test
10	6,927,471	Electronic system modules and method of fabrication
11	6,881,609	Component connections using bumps and wells
12	6,309,049	Printing apparatus and method for imaging charged toner particles using direct writing methods
13	5,400,062	Electrostatic printing apparatus and method
14	5,287,127	Electrostatic printing apparatus and method
15	5,153,617	Digitally controlled method and apparatus for delivering toners to substrates
16	5,030,976	Electrodielectric printing apparatus and process
17	RE32,897	Thermal print head
18	4,777,500	Electrostatic color printer
19	4,733,256	Electrostatic color printer
20	4,259,676	Thermal print head
21	4,169,262	Video display circuit for games, or the like

